

5

4

3

2

1

VERSION HISTORY

D

C

B

A

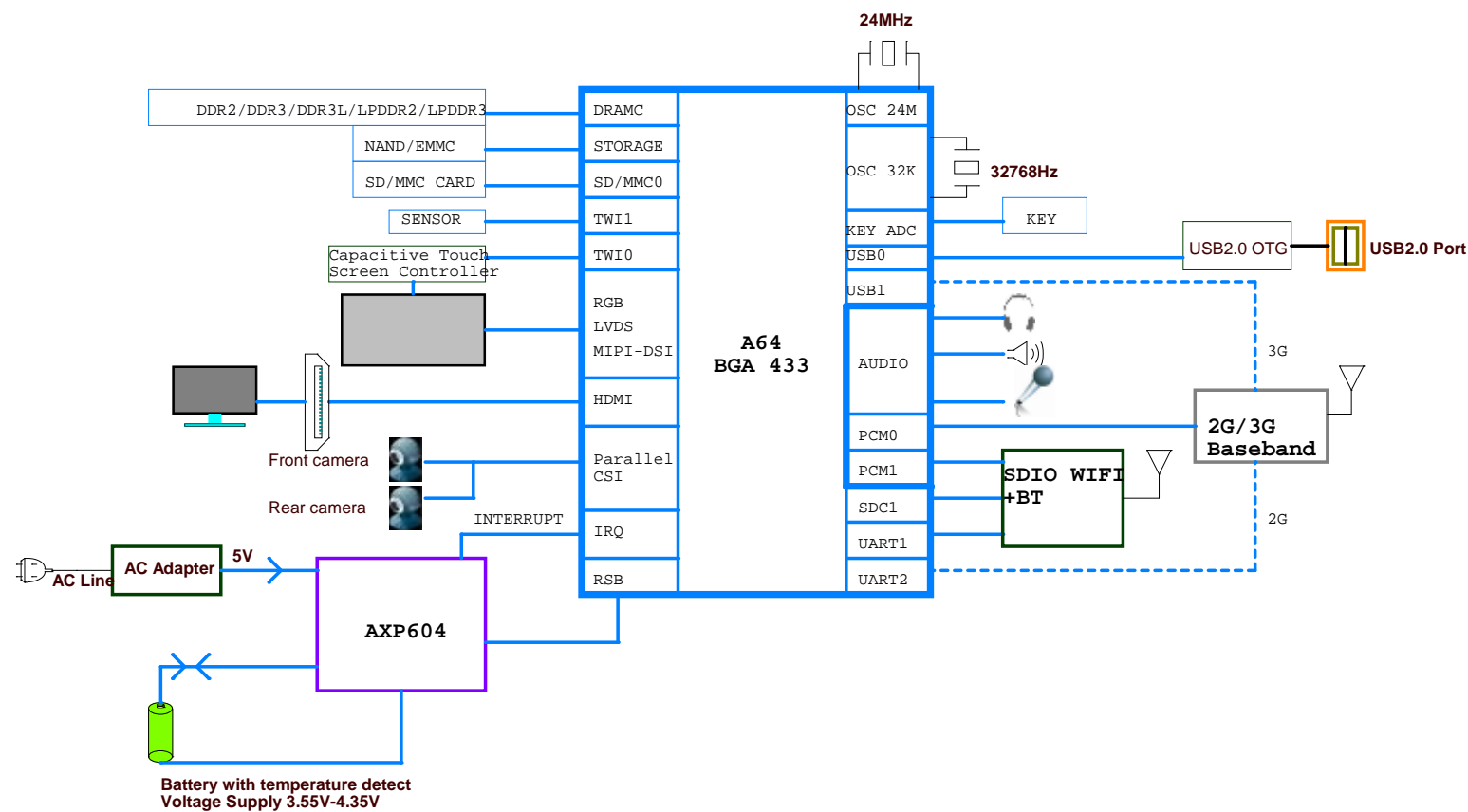
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Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Releas version	2015-04-22			

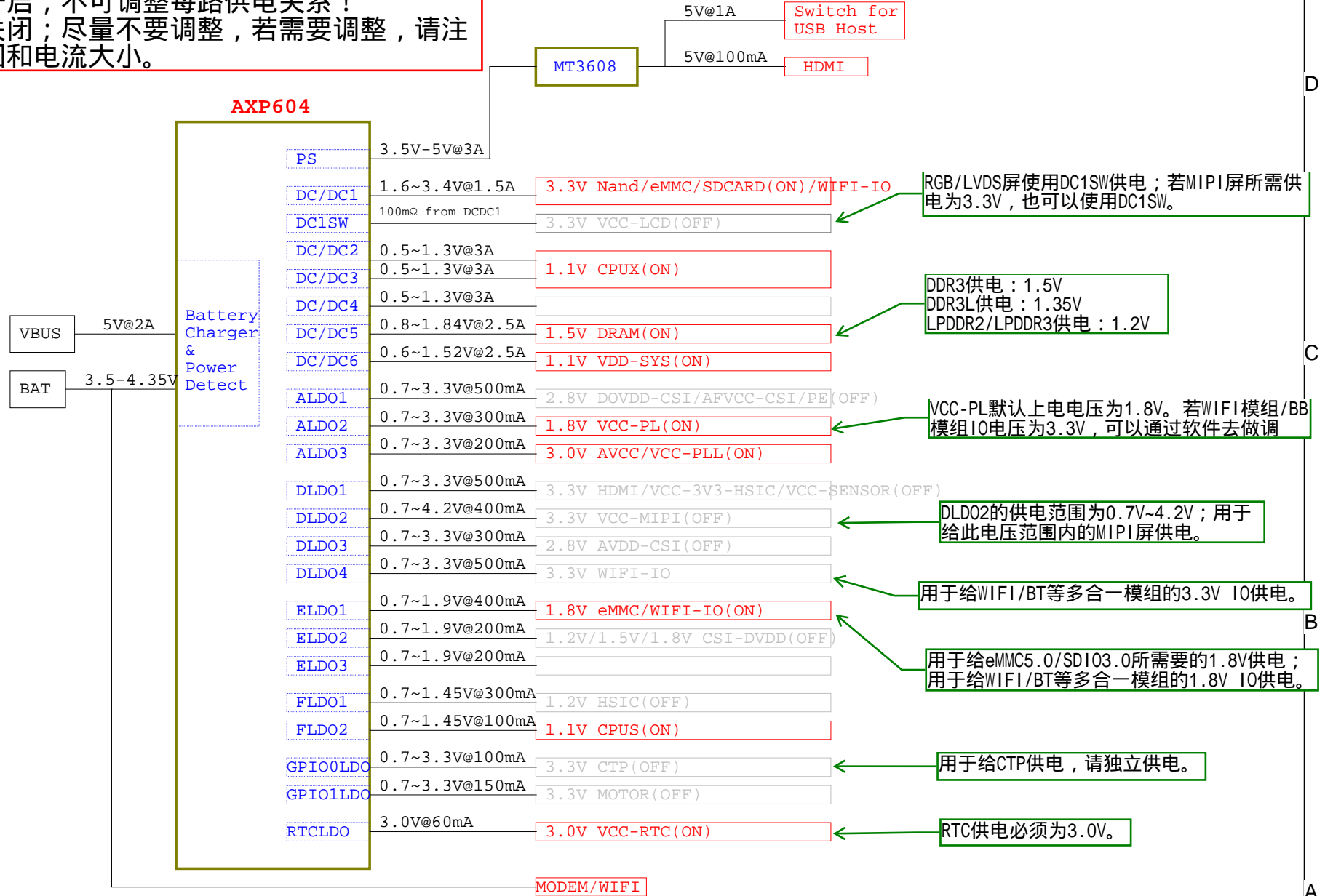
原理图设计说明V1.0

BLOCK DIAGRAM



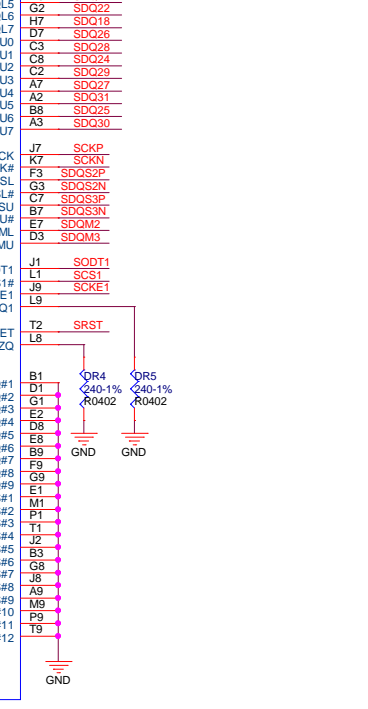
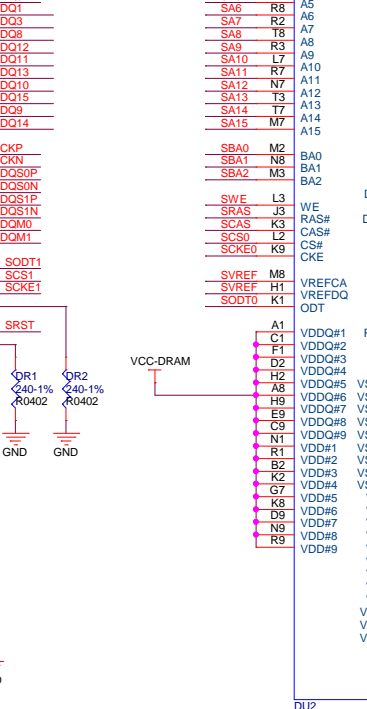
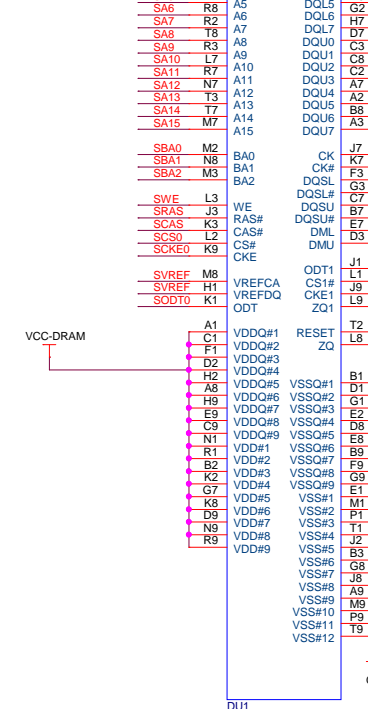
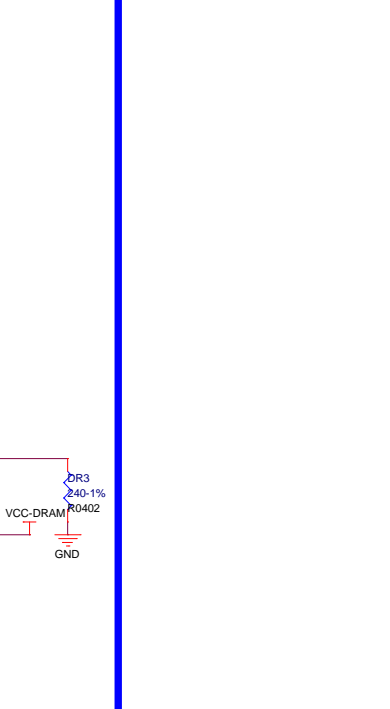
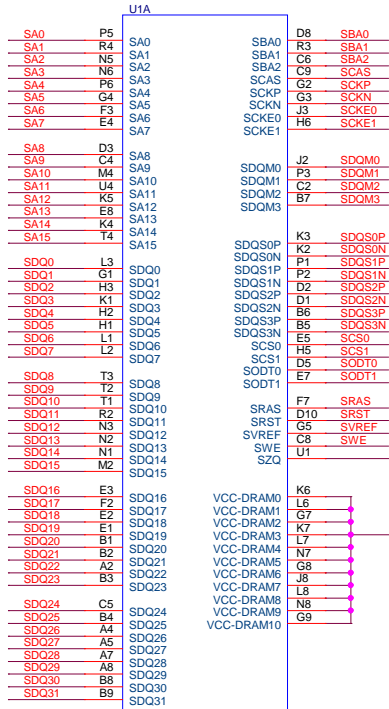
POWER TREE

红色：上电默认开启，不可调整每路供电关系！
灰色：上电默认关闭；尽量不要调整，若需要调整，请注意每一路电压范围和电流大小。

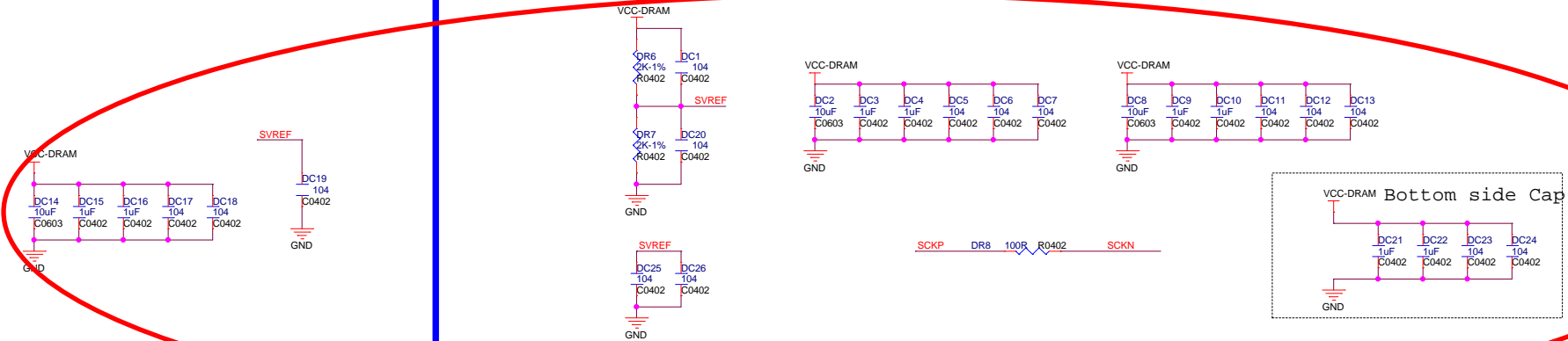


DDR3 16x2

请尽量使用Allwinner提供的DDR Layout参考模板；否则请严格遵守DDR Layout Guide。



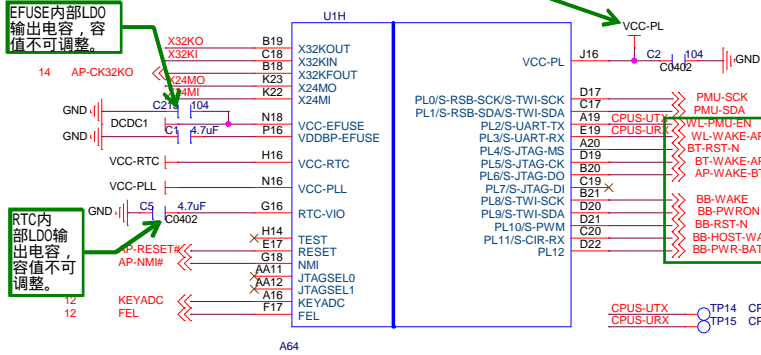
采用Allwinner DDR Layout模板，红色框中的元器件位号不能变。



CPU

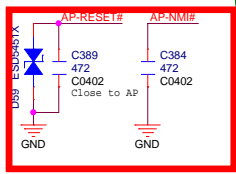
VCC-PL的电压根据WIFI模组/BB基带的IO电压进行调整；默认为1.8V，可调整为3.3V。

EFUSE内部LDO输出电容，容值不可调整。



WIFI模组/BB基带的控制信号，控制关系尽量不要调整。

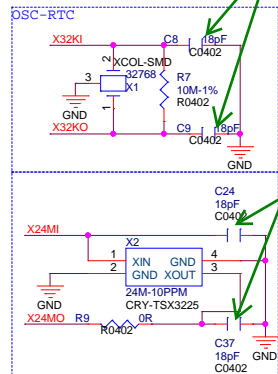
远离板边及敏感信号，包地处理。



HPOUTL/HPOUTR走线宽度不小于8mil。

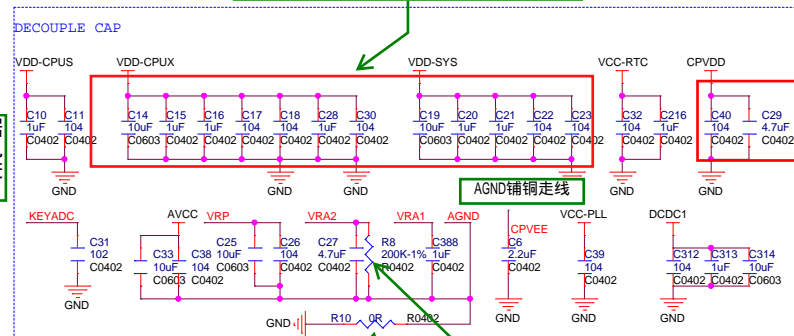
≥8mil

容值可根据晶体负载电容的大小进行调整！



容值可根据晶体负载电容的大小进行调整！

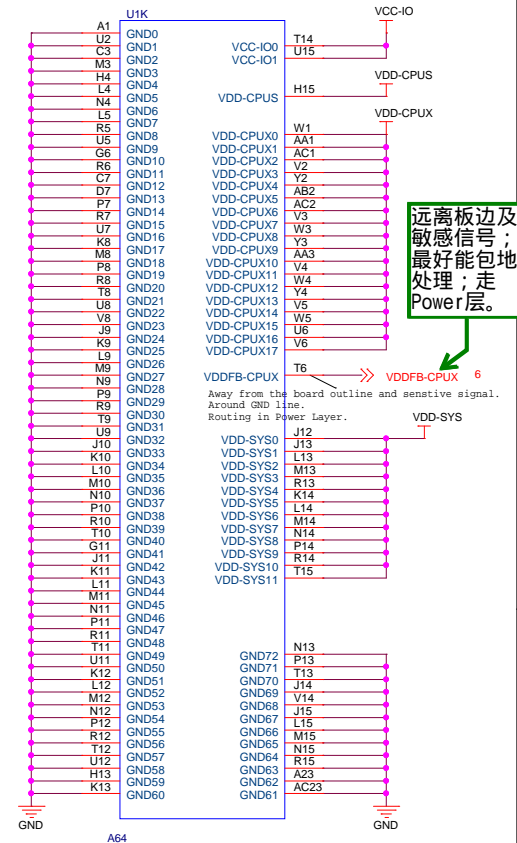
为了保证系统的稳定性，电容的数量和容值大小尽量不要改动！



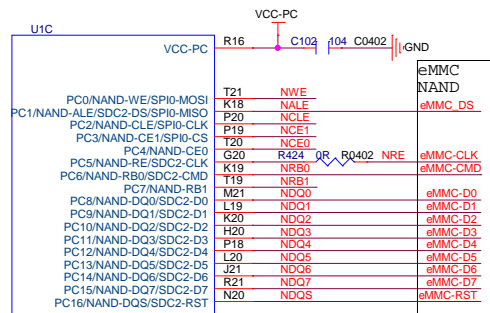
AGND与GND单点连接！

R8电阻精度为1%，阻值不可调！

远离板边及敏感信号；最好能包地处理；走Power层。



NAND/eMMC



A64



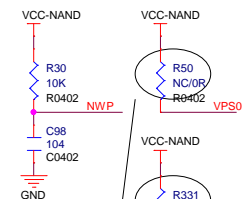
当使用的Flash IO口电压为
1.8V, D框中元件要贴;
当使用的Flash IO口电压为
3.3V, D框中元件NC.

If use eMMC 5.0, mount D.
else, NC D.

Both eMMC NAND and first TSOP NAND layout together

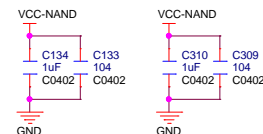
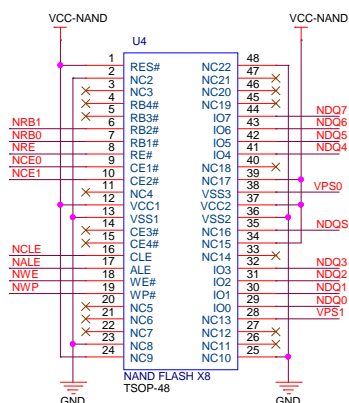
- (1) 1 NAND : [1 CE or 2 CE]
- (2) 2 NAND : [1 CE]

贴一片NAND, 可以是1 CE或2 CE ;
贴两片NAND, 两片都为1 CE。

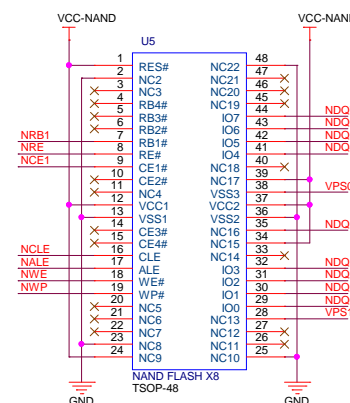


Please mount this two resistors if use
Sandisk or Toshiba nand flash

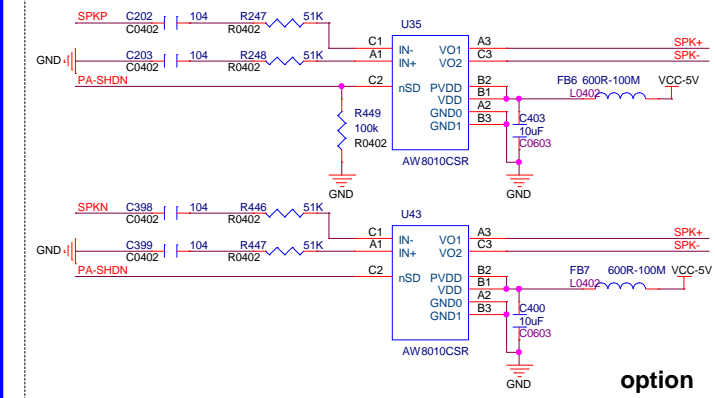
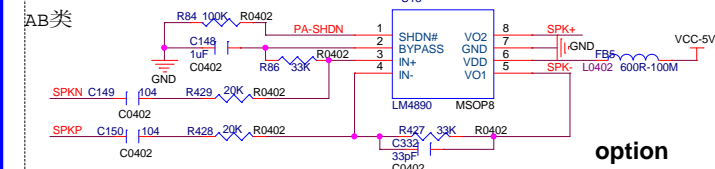
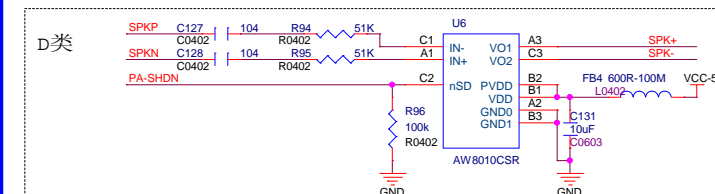
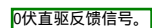
The first NAND FLASH



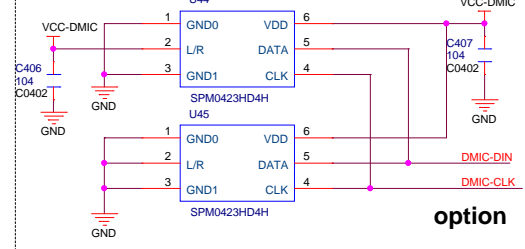
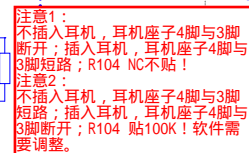
The second NAND FLASH



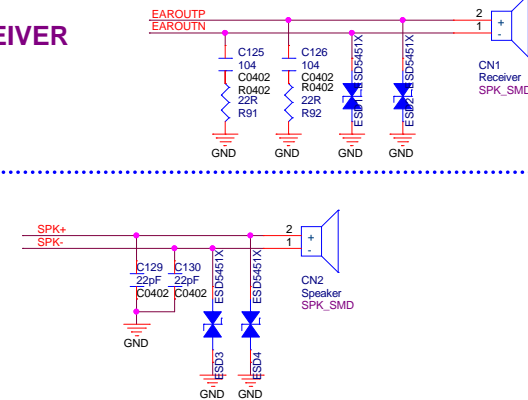
HP_JACK



ECM AMIC

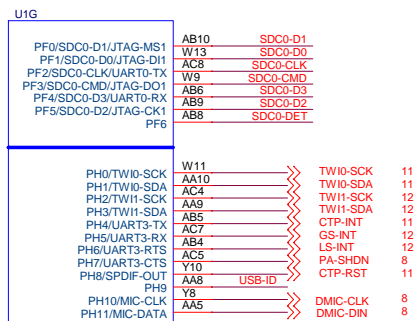
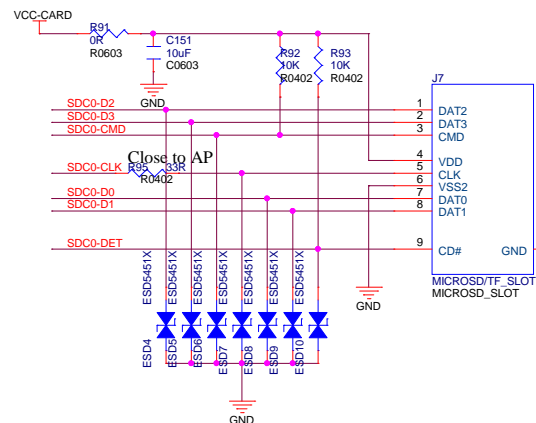


RECEIVER



T-CADD/USB

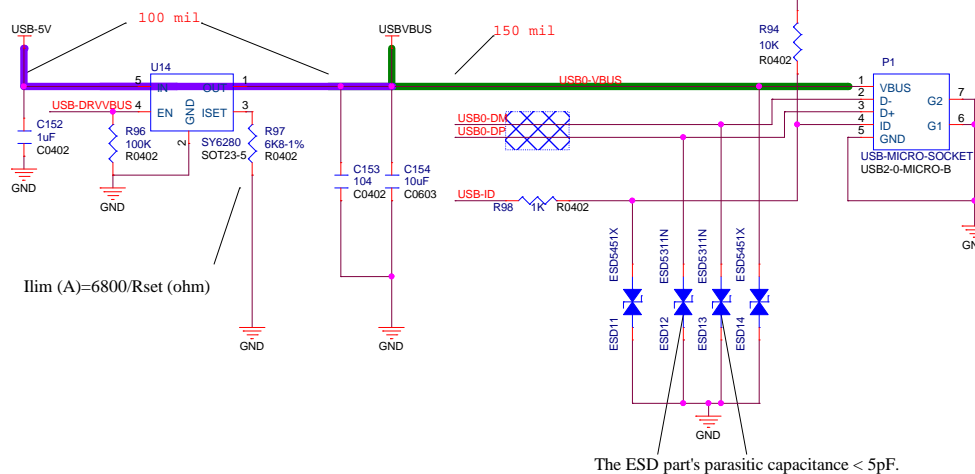
T-CARD



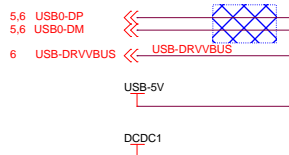
A64

VCC-CARD

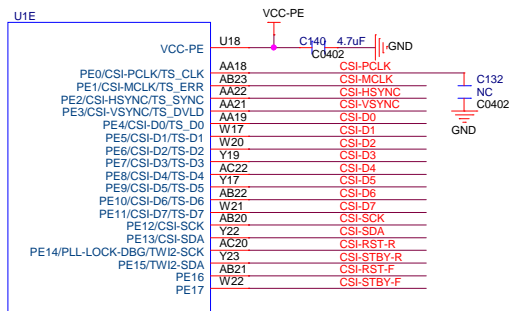
USB



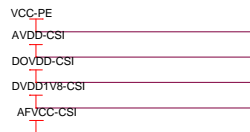
The ESD part's parasitic capacitance $< 5\text{pF}$.



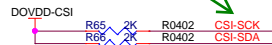
CAMREA



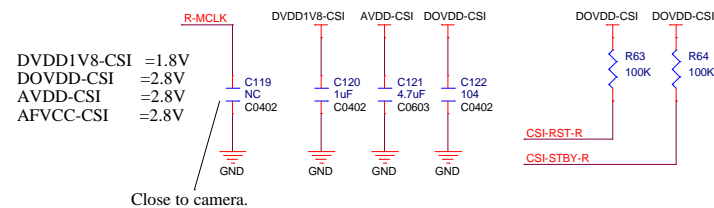
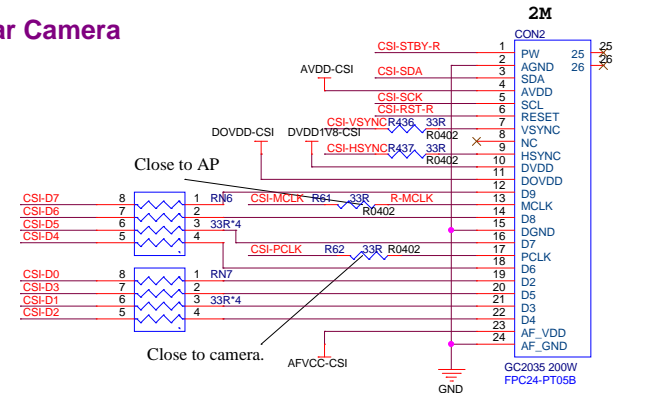
A64



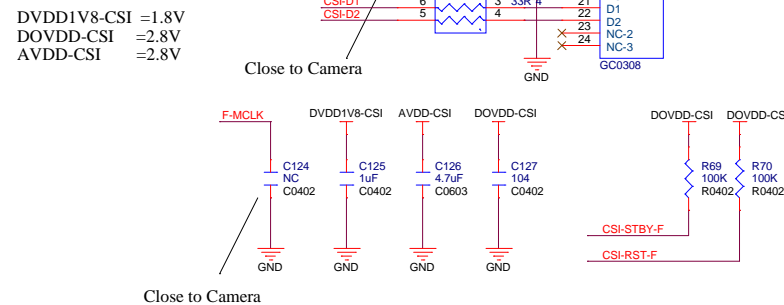
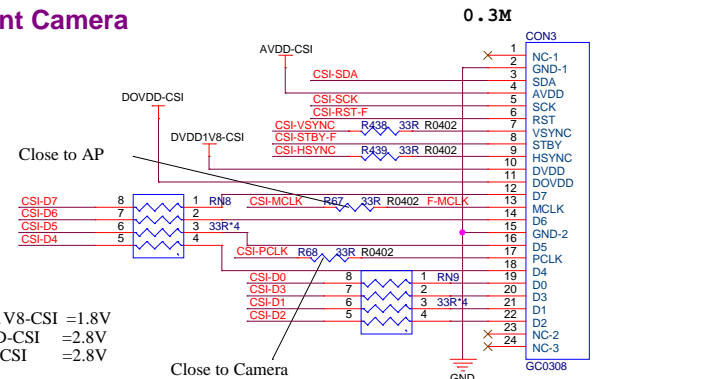
Camera的I2C不要和其它器件复用。



Rear Camera



Front Camera



AllWinner Technology Co.,Ltd

Design Name

A64-STD

Size

A3

Page Name

CAMREA

Rev

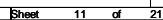
Date

Tuesday, May 12, 2015

Sheet

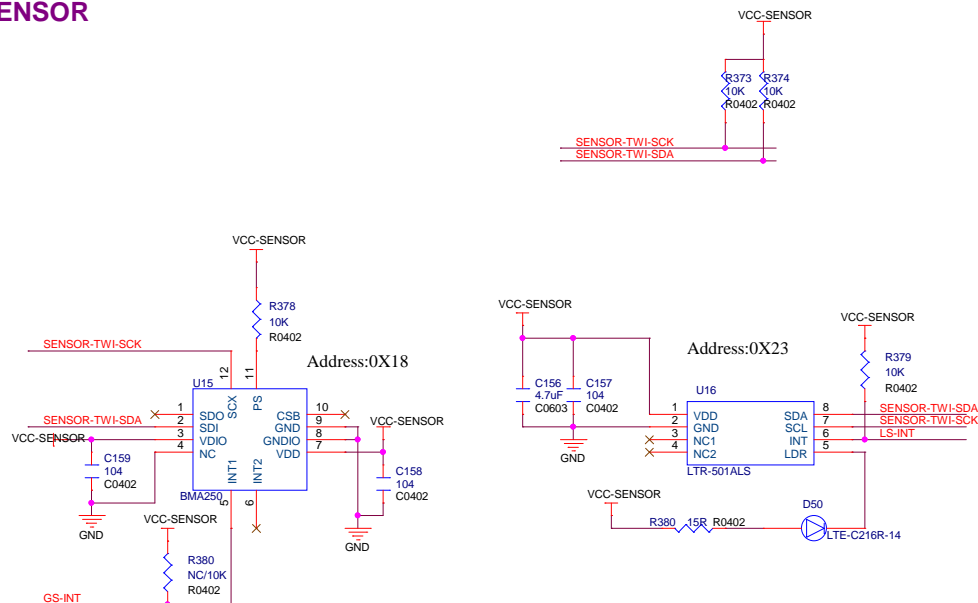
10 of 21

1



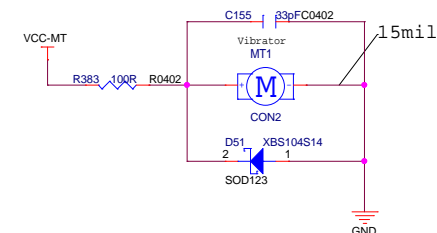
SENSORs/MT/KEY

SENSOR

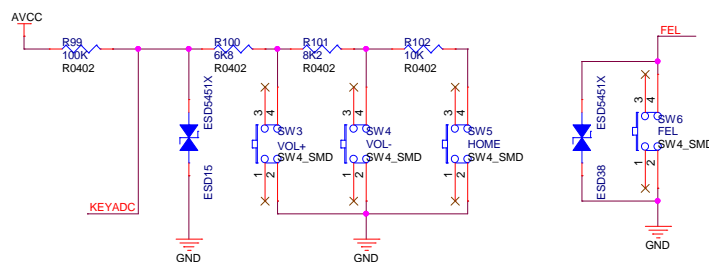


place PIN1 in the top right, parallel to the screen,
and put on the top left of the screen

Motor

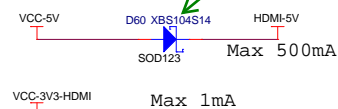


KEY



HDMI

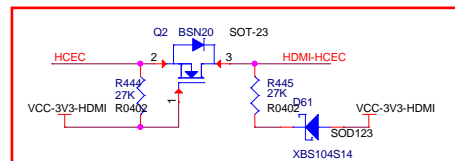
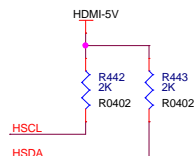
5 HTX0P
5 HTX0N
5 HTX1P
5 HTX1N
5 HTX2P
5 HTX2N
5 HTXCP
5 HTXCN
5 HHPD
5 HCEC
5 HSCL
5 HSDA



防止接入HDMI时，在系统待机状态下向系统倒灌电。

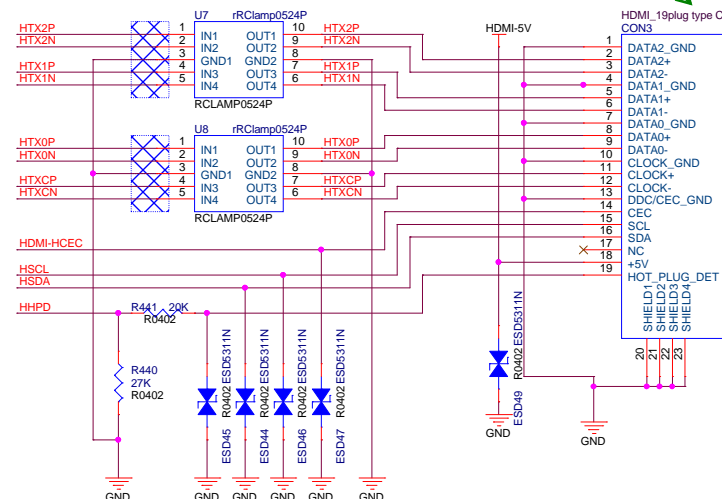


Differential pairs
Z0= 100 ohm



防止接入HDMI时，在系统待机状态下向系统倒灌电；若不需要CEC功能，该电路可不贴，HDMI-HCEC信号悬空。

在做原理图设计时，请注意HDMI座的型号，型号不同，线序不同，请注意！



A



1

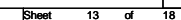


B

AP6210, Mount A+C+D+E, NC B+F
AP6181, Mount B+E, NC A+C+D+F
8723BS, Mount F, NC A+B+C+D+E
AP6330/6335, Mount B+C+E, NC A+D+F



USB WIFI



2



2

A

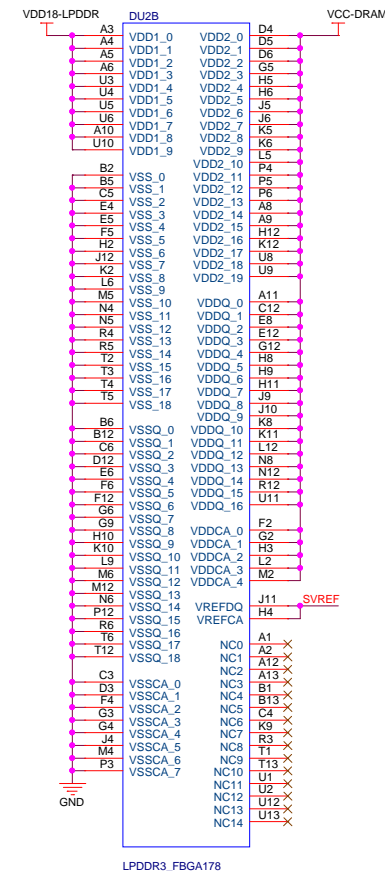
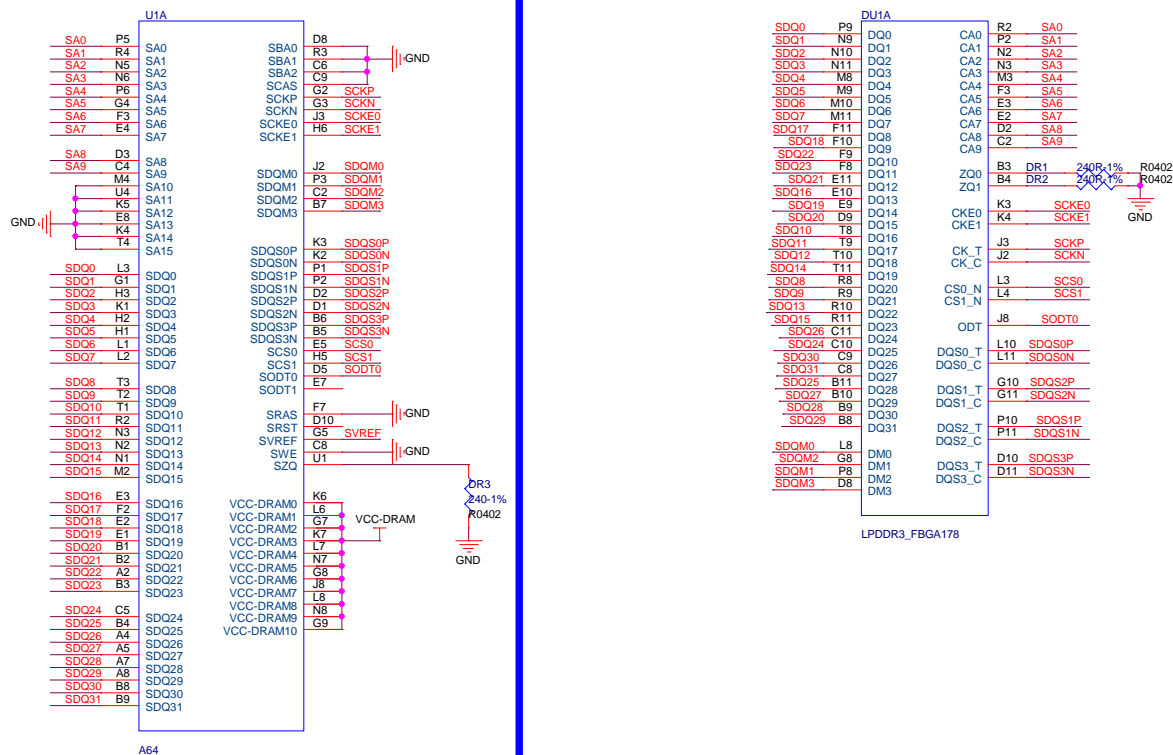


POW

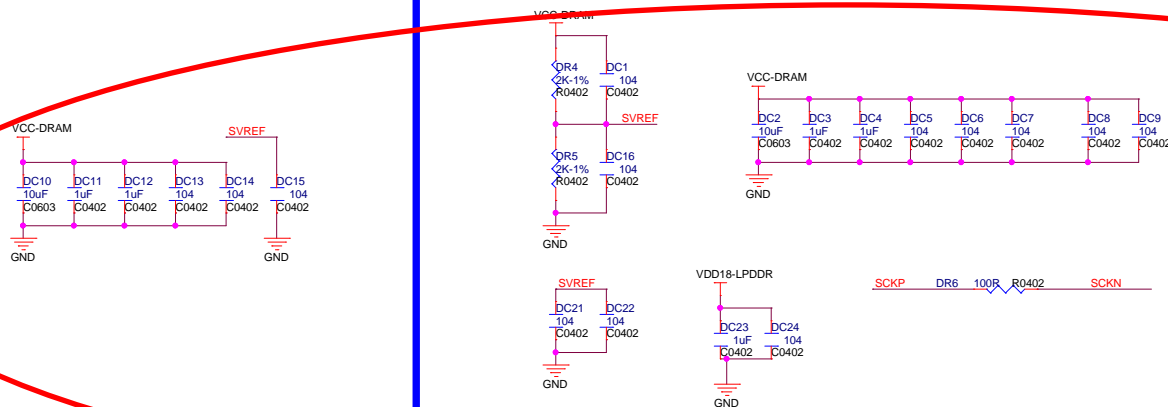


LPDDR3

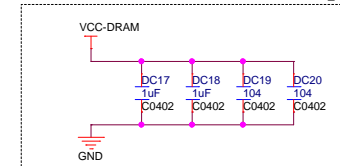
请尽量使用Allwinner提供的DDR Layout参考模板；否则请严格遵守DDR Layout Guide。



采用Allwinner DDR Layout模板，红色框中的元器件位号不能变。



Bottom side Cap

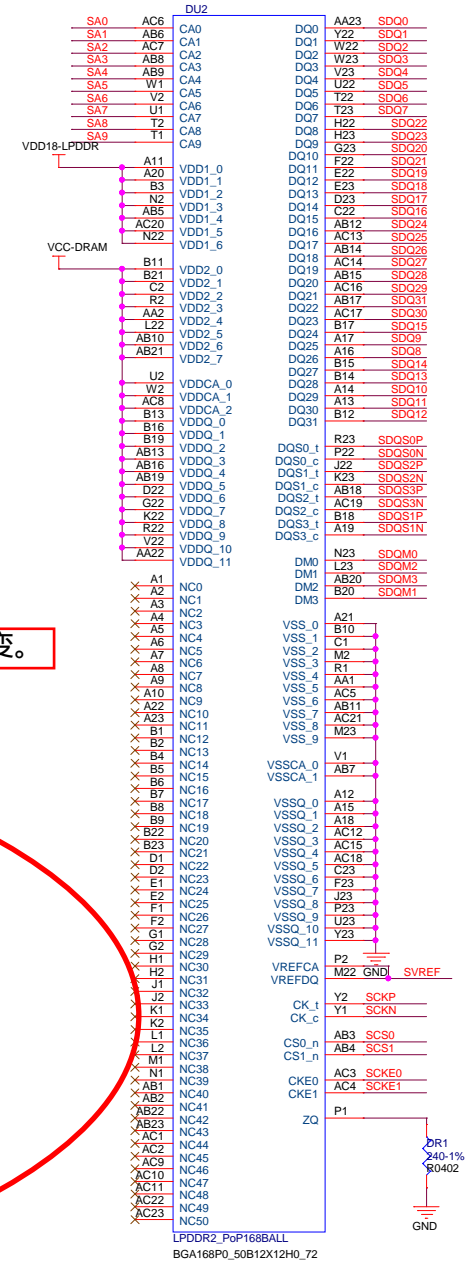
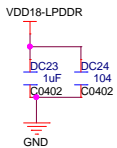
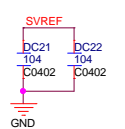
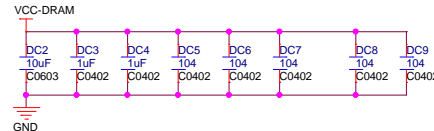
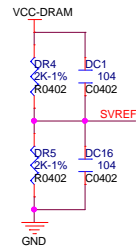
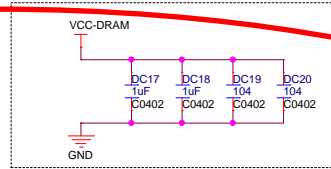
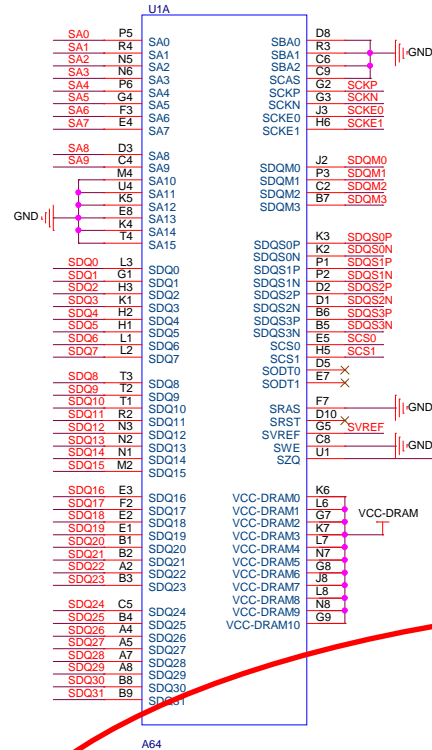


LPDDR3/LPDDR2

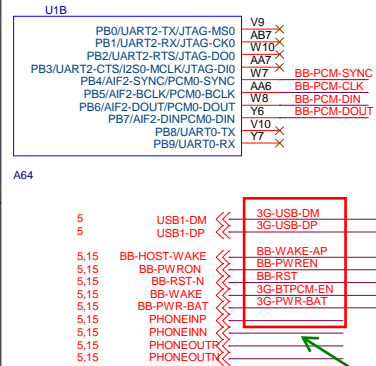
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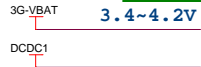
Bottom side Cap



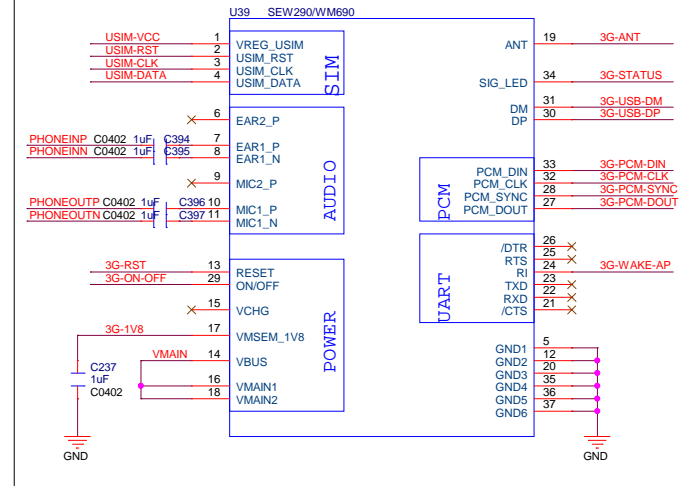
MODEM 3G



模组10电压为2.8V~3.3V, 若VCC-PL电压为1.8V, 则需要进行10电平转换!

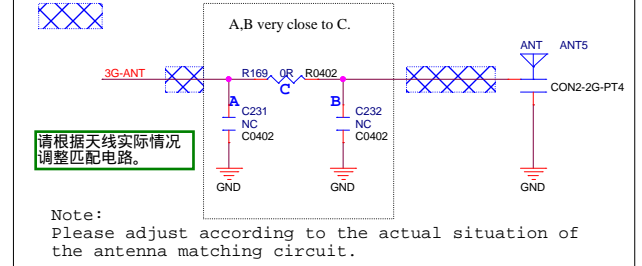


Modem

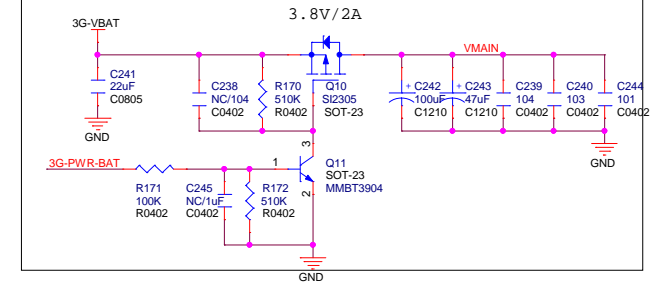


RF

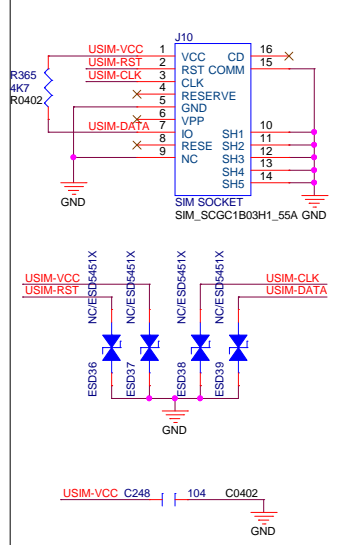
50 ohm



POWER

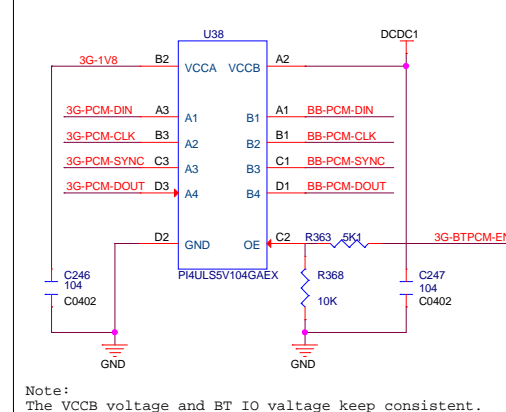


USIM



LEVEL TRANSFORM

Note:
VCCB>VCCA.



CTRL

