



= Short Datasheet =

AK8963

## 3-axis Electronic Compass

### 1. Features

A 3-axis electronic compass IC with high sensitive Hall sensor technology.  
Best adapted to pedestrian city navigation use for cell phone and other portable appliance.

Functions:

- 3-axis magnetometer device suitable for compass application
- Built-in A to D Converter for magnetometer data out
- 14-/16-bit selectable data out for each 3 axis magnetic components
  - Sensitivity: 0.6  $\mu$ T/LSB typ. (14-bit)
  - 0.15 $\mu$ T/LSB typ. (16-bit)
- Serial interface
  - I<sup>2</sup>C bus interface.
    - Standard mode and Fast mode compliant with Philips I<sup>2</sup>C specification Ver.2.1
  - 4-wire SPI
- Operation modes:
  - Power-down, Single measurement, Continuous measurement, External trigger measurement, Self test and Fuse ROM access.
- DRDY function for measurement data ready
- Magnetic sensor overflow monitor function
- Built-in oscillator for internal clock source
- Power on Reset circuit
- Self test function with built-in internal magnetic source

Operating temperatures:

- -30°C to +85°C

Operating supply voltage:

- Analog power supply +2.4V to +3.6V
- Digital Interface supply +1.65V to analog power supply voltage.

Current consumption:

- Power-down: 3  $\mu$ A typ.
- Measurement:
  - Average power consumption at 8 Hz repetition rate: 280 $\mu$ A typ.

Package:

AK8963C	14-pin WL-CSP (BGA):	1.6 mm ´ 1.6 mm ´ 0.5 mm (typ.)
AK8963N	16-pin QFN package:	3.0 mm ´ 3.0 mm ´ 0.75 mm (typ.)

## 2. Overview

AK8963 is 3-axis electronic compass IC with high sensitive Hall sensor technology.

Small package of AK8963 incorporates magnetic sensors for detecting terrestrial magnetism in the X-axis, Y-axis, and Z-axis, a sensor driving circuit, signal amplifier chain, and an arithmetic circuit for processing the signal from each sensor. Self test function is also incorporated. From its compact foot print and thin package feature, it is suitable for map heading up purpose in GPS-equipped cell phone to realize pedestrian navigation function.

AK8963 has the following features:

- (1) Silicon monolithic Hall-effect magnetic sensor with magnetic concentrator realizes 3-axis magnetometer on a silicon chip. Analog circuit, digital logic, power block and interface block are also integrated on a chip.
- (2) Wide dynamic measurement range and high resolution with lower current consumption.
 

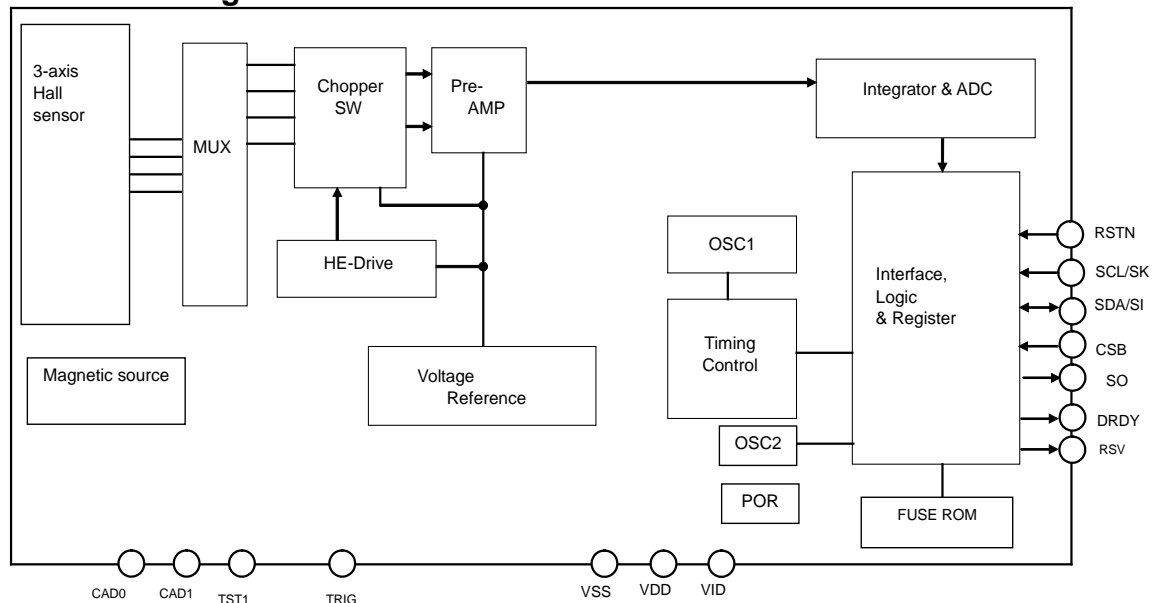
Output data resolution:	14-bit (0.6 $\mu$ T/LSB)
	16-bit (0.15 $\mu$ T/LSB)
Measurement range:	$\pm$ 4900 $\mu$ T
Average current at 8Hz repetition rate:	280 $\mu$ A typ.
- (3) Digital serial interface
  - I<sup>2</sup>C bus interface to control AK8963 functions and to read out the measured data by external CPU. A dedicated power supply for I<sup>2</sup>C bus interface can work in low-voltage apply as low as 1.65V.
  - 4-wire SPI is also supported. A dedicated power supply for SPI can work in low-voltage apply as low as 1.65V.
- (4) DRDY pin and register inform to system that measurement is end and set of data in registers are ready to be read.
- (5) Device is worked by on-chip oscillator so no external clock source is necessary.
- (6) Self test function with internal magnetic source to confirm magnetic sensor operation on end products.

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## 4. Circuit Configuration

### 4.1. Block Diagram



### 4.2. Block Function

Block	Function
3-axis Hall sensor	Monolithic Hall elements.
MUX	Multiplexer for selecting Hall elements.
Chopper SW	Performs chopping.
HE-Drive	Magnetic sensor drive circuit for constant-current driving of sensor
Pre-AMP	Fixed-gain differential amplifier used to amplify the magnetic sensor signal.
Integrator & ADC	Integrates and amplifies pre-AMP output and performs analog-to-digital conversion.
OSC1	Generates an operating clock for sensor measurement. 12MHz(typ.)
OSC2	Generates an operating clock for sequencer. 128kHz(typ.)
POR	Power On Reset circuit. Generates reset signal on rising edge of VDD.
Interface Logic & Register	Exchanges data with an external CPU. DRDY pin indicates sensor measurement end and data is ready to be read. I <sup>2</sup> C bus interface using two pins, namely, SCL and SDA. Standard mode and Fast mode are supported. The low-voltage specification can be supported by applying 1.65V to the VID pin. 4-wire SPI is also supported by SK, SI, SO and CSB pins. 4-wire SPI works in VID pin voltage down to 1.65V, too.
Timing Control	Generates a timing signal required for internal operation from a clock generated by the OSC1.
Magnetic Source	Generates magnetic field for self test of magnetic sensor.
FUSE ROM	Fuse for adjustment

## 4.3. Pin Function

QFN Pin No.	WLCSP Pin No.	Pin name	I/O	Power supply system	Type	Function
1	A1	DRDY	O	VID	CMOS	Data Ready output pin. "H" active. Informs measurement ended and data is ready to be read.
2	A2	CSB	I	VID	CMOS	Chip select pin for 4-wire SPI. "L" active. Connect to VID when selecting I <sup>2</sup> C bus interface.
3	A3	SCL	I	VID	CMOS	When the I <sup>2</sup> C bus interface is selected (CSB pin is connected to VID) SCL: Control data clock input pin Input: Schmidt trigger
		SK				When the 4-wire SPI is selected SK: Serial clock input pin
5	A4	SDA	I/O	VID	CMOS	When the I <sup>2</sup> C bus interface is selected (CSB pin is connected to VID) SDA: Control data input/output pin Input: Schmidt trigger, Output: Open drain
		SI	I			When the 4-wire SPI is selected SI: Serial data input pin
15	B1	VDD	-	-	Power	Analog Power supply pin.
4	B3	RSV	O	VID	CMOS	Reserved. Keep this pin electrically non-connected.
6	B4	SO	O	VID	CMOS	When the I <sup>2</sup> C bus interface is selected (CSB pin is connected to VID) Hi-Z output. Keep this pin electrically non-connected.
						When the 4-wire SPI is selected Serial data output pin
13	C1	VSS	-	-	Power	Ground pin.
14	C2	TST1	I	VDD	CMOS	Test pin. Pulled down by 100kΩ internal resistor. Keep this pin electrically non-connected or connect to VSS.
7	C3	TRG	I	VID	CMOS	External trigger pulse input pin. Enabled only in External trigger mode. Pulled down by 100kΩ internal resistor. When External trigger mode is not in use, keep this pin electrically non-connected or connect to VSS.
8	C4	VID	-	-	Power	Digital interface positive power supply pin.
12	D1	CAD0	I	VDD	CMOS	When the I <sup>2</sup> C bus interface is selected (CSB pin is connected to VID) CAD0: Slave address 0 input pin Connect to VSS or VDD.
						When the 4-wire serial interface is selected Connect to VSS.
11	D2	CAD1	I	VDD	CMOS	When the I <sup>2</sup> C bus interface is selected (CSB pin is connected to VID) CAD1: Slave address 1 input pin Connect to VSS or VDD.
						When the 4-wire serial interface is selected Connect to VSS.
10	D4	RSTN	I	VID	CMOS	Reset pin. Resets registers by setting to "L". Connect to VID when not in use.

## 5. Overall Characteristics

### 5.1. Absolute Maximum Ratings

V<sub>SS</sub>=0V

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage (V <sub>DD</sub> , V <sub>ID</sub> )	V+	-0.3	+4.3	V
Input voltage	V <sub>IN</sub>	-0.3	(V <sub>+</sub> )+0.3	V
Input current	I <sub>IN</sub>	-	±10	mA
Storage temperature	T <sub>ST</sub>	-40	+125	°C

(Note 1) If the device is used in conditions exceeding these values, the device may be destroyed. Normal operations are not guaranteed in such exceeding conditions.

### 5.2. Recommended Operating Conditions

V<sub>SS</sub>=0V

Parameter	Remark	Symbol	Min.	Typ.	Max.	Unit
Operating temperature		T <sub>a</sub>	-30		+85	°C
Power supply voltage	V <sub>DD</sub> pin voltage	V <sub>DD</sub>	2.4	3.0	3.6	V
	V <sub>ID</sub> pin voltage	V <sub>ID</sub>	1.65		V <sub>DD</sub>	V

### 5.3. Electrical Characteristics

The following conditions apply unless otherwise noted:

V<sub>DD</sub>=2.4V to 3.6V, V<sub>ID</sub>=1.65V to V<sub>DD</sub>, Temperature range=-30°C to 85°C

#### 5.3.1. DC Characteristics

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level input voltage 1	V <sub>IH1</sub>	CSB		70%V <sub>ID</sub>			V
Low level input voltage 1	V <sub>IL1</sub>	RSTN TRG				30%V <sub>ID</sub>	V
High level input voltage 2	V <sub>IH2</sub>	SK/SCL		70%V <sub>ID</sub>		V <sub>ID</sub> +0.5	V
Low level input voltage 2	V <sub>IL2</sub>	SI/SDA		-0.5		30%V <sub>ID</sub>	V
High level input voltage 3	V <sub>IH3</sub>	CAD0		70%V <sub>DD</sub>			V
Low level input voltage 3	V <sub>IL3</sub>	CAD1				30%V <sub>DD</sub>	V
Input current 1	I <sub>IN1</sub>	SK/SCL SI/SDA CSB RSTN	V <sub>IN</sub> =V <sub>SS</sub> or V <sub>ID</sub>	-10		+10	mA
Input current 2	I <sub>IN2</sub>	CAD0 CAD1	V <sub>IN</sub> =V <sub>SS</sub> or V <sub>DD</sub>	-10		+10	mA
Input current 3	I <sub>IN3</sub>	TRG	V <sub>IN</sub> =V <sub>ID</sub>			100	mA
Input current 4	I <sub>IN4</sub>	TST1	V <sub>IN</sub> =V <sub>DD</sub>			100	mA
Hysteresis input voltage (Note 2)	V <sub>HS</sub>	SCL SDA	V <sub>ID</sub> ≥2V	5%V <sub>ID</sub>			V
			V <sub>ID</sub> <2V	10%V <sub>ID</sub>			V
High level output voltage 1	V <sub>OH1</sub>	SO	I <sub>OH</sub> <sup>3</sup> -100μA	80%V <sub>ID</sub>			V
Low level output voltage 1	V <sub>OL1</sub>	DRDY	I <sub>OL</sub> ≤+100μA			20%V <sub>ID</sub>	V
Low level output voltage 2 (Note 3)(Note 4)	V <sub>OL2</sub>	SDA	I <sub>OL</sub> ≤3mA V <sub>ID</sub> ≥2V			0.4	V
			I <sub>OL</sub> ≤3mA V <sub>ID</sub> <2V			20%V <sub>ID</sub>	V
Current consumption (Note 5)	IDD1	V <sub>DD</sub> V <sub>ID</sub>	Power-down mode V <sub>DD</sub> =V <sub>ID</sub> =3.0V		3	10	mA
	IDD2		When magnetic sensor is driven		5	10	mA
	IDD3		Self-test mode		9	15	mA
	IDD4		(Note 6)		0.1	5	mA

(Note 2) Schmitt trigger input (reference value for design)

(Note 3) Maximum load capacitance: 400pF (capacitive load of each bus line applied to the I<sup>2</sup>C bus interface)

(Note 4) Output is open-drain. Connect a pull-up resistor externally.

(Note 5) Without any resistance load

(Note 6) (case1)V<sub>DD</sub>=ON, V<sub>ID</sub>=ON, RSTN pin = "L". (case2)V<sub>DD</sub>=ON, V<sub>ID</sub>=OFF(0V), RSTN pin = "L".

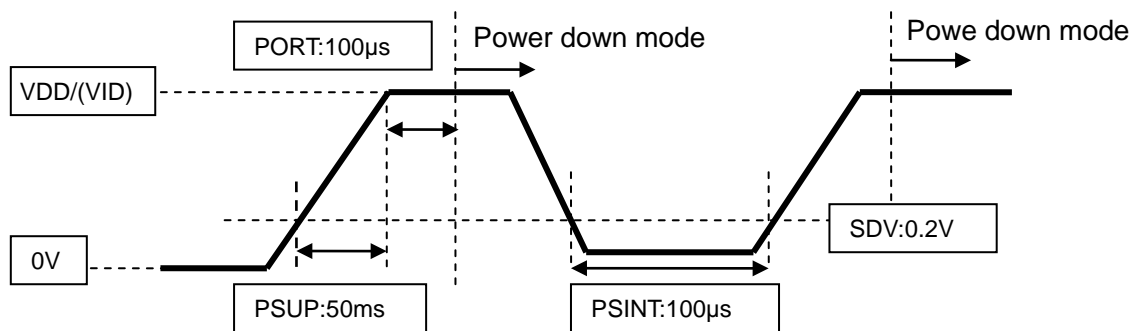
(case3)Vdd=Off(0V), Vid=On.

**5.3.2. AC Characteristics**

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Power supply rise time (Note 7)	PSUP	VDD VID	Period of time that VDD (VID) changes from 0.2V to Vdd (Vid). (Note 8)			50	ms
POR completion time (Note 7)	PORT		Period of time after PSUP to Power-down mode (Note 8)			100	$\mu$ s
Power supply turn off voltage	SDV	VDD VID	Turn off voltage to enable POR to restart (Note 8)			0.2	V
Power supply turn on interval (Note 7)	PSINT	VDD VID	Period of time that voltage lower than SDV needed to be kept to enable POR to restart (Note 8)	100			$\mu$ s
Wait time before mode setting	Twat			100			ms

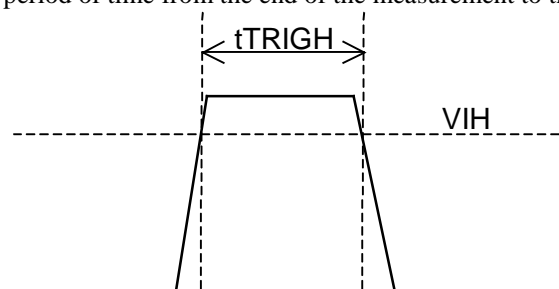
(Note 7) Reference value for design

(Note 8) When POR circuit detects the rise of VDD/VID voltage, it resets internal circuits and initializes the registers. After reset, AK8963 transits to Power-down mode.

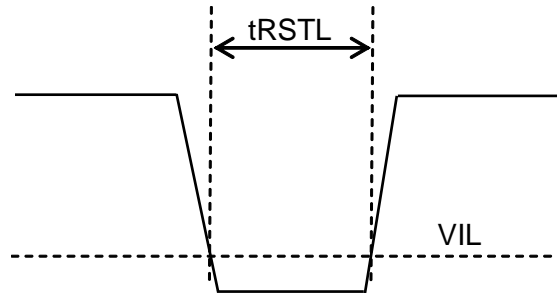


Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Trigger input effective pulse width	tTRIGH	TRG		200			ns
Trigger input effective frequency (Note 9)	tTRIGf	TRG				100	Hz

(Note 9) The value when the period of time from the end of the measurement to the next trigger input is 1.3ms.



Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Reset input effective pulse width ("L")	tRSTL	RSTN		5			ms



### 5.3.3. Analog Circuit Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Measurement data output bit	DBIT	BIT = "0"		14		bit
		BIT = "1"		16		
Time for measurement	TSM	Single measurement mode		7.2	9	ms
Magnetic sensor sensitivity	BSE	Tc=25°C (Note 10)				mT/LSB
		BIT = "0"	0.57	0.6	0.63	
		BIT = "1"	0.1425	0.15	0.1575	
Magnetic sensor measurement range (Note 11)	BRG	Tc=25°C (Note 10)	±4912			mT
Magnetic sensor initial offset (Note 12)		Tc=25°C BIT = "0"	-500		500	LSB

(Note 10) Value after sensitivity is adjusted using sensitivity fine adjustment data stored in Fuse ROM.

(Note 11) Reference value for design

(Note 12) Value of measurement data register on shipment without applying magnetic field on purpose.



### 5.3.4. 4-wire SPI

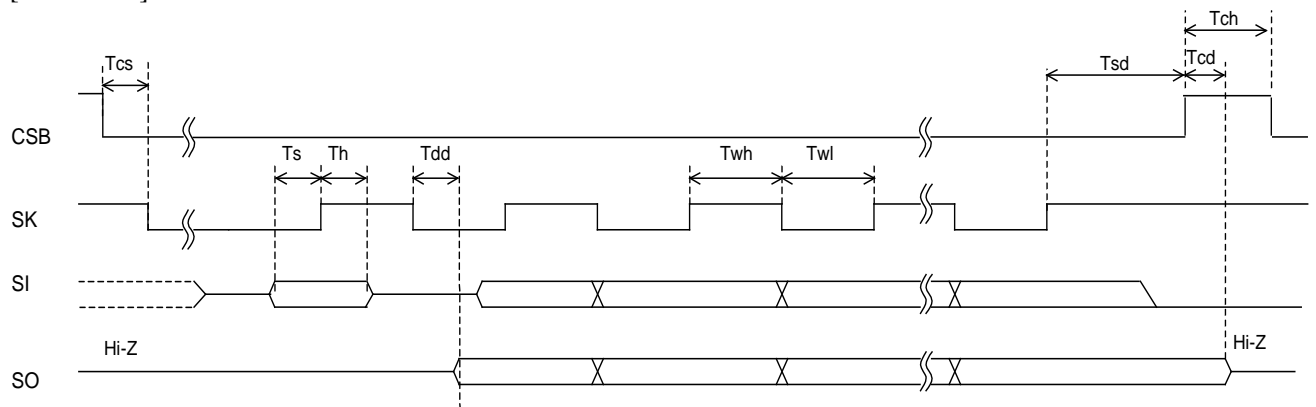
4-wire SPI is compliant with mode 3

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CSB setup time	Tcs		50			ns
Data setup time	Ts		50			ns
Data hold time	Th		50			ns
SK high time	Twh	Vid <sup>3</sup> 2.5V	100			ns
		2.5V>Vid <sup>3</sup> 1.65V	150			ns
SK low time	Twl	Vid <sup>3</sup> 2.5V	100			ns
		2.5V>Vid <sup>3</sup> 1.65V	150			ns
SK setup time	Tsd		50			ns
SK to SO delay time (Note 13)	Tdd				50	ns
CSB to SO delay time (Note 13)	Tcd				50	ns
SK rise time (Note 14)	Tr				100	ns
SK fall time (Note 14)	Tf				100	ns
CSB high time	Tch		150			ns

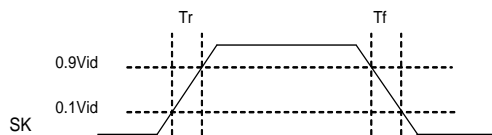
(Note 13) SO load capacitance: 20pF

(Note 14) Reference value for design.

[4-wire SPI]



[Rise time and fall time]



### 5.3.5. I<sup>2</sup>C Bus Interface

CSB pin = "H"

I<sup>2</sup>C bus interface is compliant with Standard mode and Fast mode. Standard/Fast mode is selected automatically by fSCL.

(1) Standard mode

fSCL ≤ 100kHz

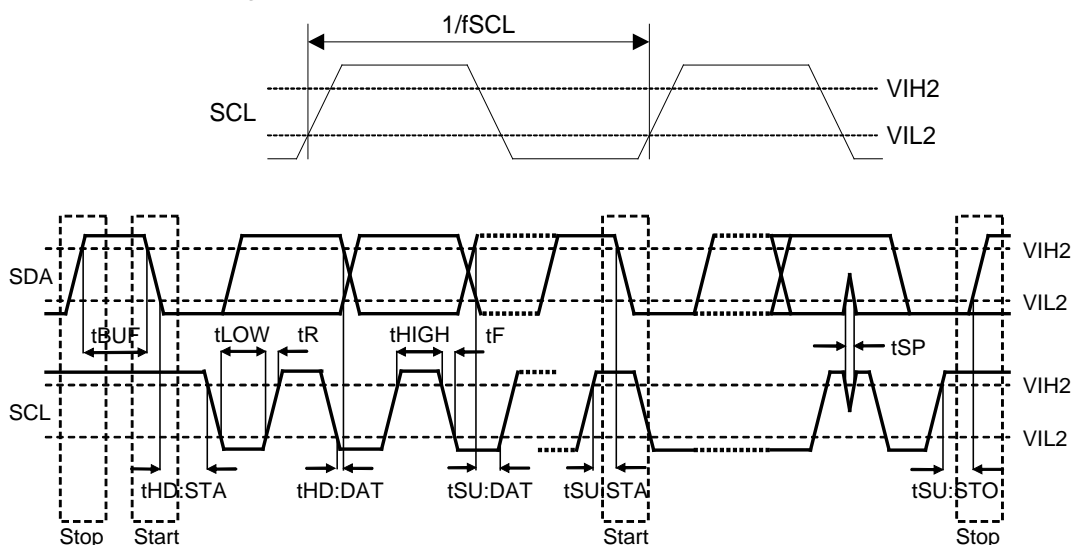
Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL clock frequency			100	kHz
t <sub>HIGH</sub>	SCL clock "High" time	4.0			µs
t <sub>LOW</sub>	SCL clock "Low" time	4.7			µs
t <sub>R</sub>	SDA and SCL rise time			1.0	µs
t <sub>F</sub>	SDA and SCL fall time			0.3	µs
t <sub>HD:STA</sub>	Start Condition hold time	4.0			µs
t <sub>SU:STA</sub>	Start Condition setup time	4.7			µs
t <sub>HD:DAT</sub>	SDA hold time (vs. SCL falling edge)	0			µs
t <sub>SU:DAT</sub>	SDA setup time (vs. SCL rising edge)	250			ns
t <sub>SU:STO</sub>	Stop Condition setup time	4.0			µs
t <sub>BUF</sub>	Bus free time	4.7			µs

(2) Fast mode

100kHz < fSCL ≤ 400kHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL clock frequency			400	kHz
t <sub>HIGH</sub>	SCL clock "High" time	0.6			µs
t <sub>LOW</sub>	SCL clock "Low" time	1.3			µs
t <sub>R</sub>	SDA and SCL rise time			0.3	µs
t <sub>F</sub>	SDA and SCL fall time			0.3	µs
t <sub>HD:STA</sub>	Start Condition hold time	0.6			µs
t <sub>SU:STA</sub>	Start Condition setup time	0.6			µs
t <sub>HD:DAT</sub>	SDA hold time (vs. SCL falling edge)	0			µs
t <sub>SU:DAT</sub>	SDA setup time (vs. SCL rising edge)	100			ns
t <sub>SU:STO</sub>	Stop Condition setup time	0.6			µs
t <sub>BUF</sub>	Bus free time	1.3			µs
t <sub>SP</sub>	Noise suppression pulse width			50	ns

[I<sup>2</sup>C bus interface timing]



## 6. Functional Explanation

### 6.1. Power States

When VDD and VID are turned on from Vdd=OFF (0V) and Vid=OFF (0V), all registers in AK8963 are initialized by POR circuit and AK8963 transits to Power-down mode.

All the states in the table below can be set, although the transition from state 2 to state 3 and the transition from state 3 to state 2 are prohibited.

Table 6.1

State	VDD	VID	Power state
1	OFF (0V)	OFF (0V)	OFF (0V). It doesn't affect external interface. Digital input pins other than SCL and SDA pin should be fixed to "L"(0V).
2	OFF (0V)	1.65V to 3.6V	OFF (0V). It doesn't affect external interface.
3	2.4V to 3.6V	OFF (0V)	OFF (0V). It doesn't affect external interface. Digital input pins other than SCL and SDA pin should be fixed to "L" (0V).
4	2.4V to 3.6V	1.65V to Vdd	ON

### 6.2. Reset Functions

When the power state is ON, always keep  $Vid \leq Vdd$ .

Power-on reset (POR) works until Vdd reaches to the operation effective voltage (about 1.4V: reference value for design) on power-on sequence. After POR is deactivated, all registers are initialized and transits to power down mode.

When Vdd=2.4 ~ 3.6V, POR circuit and VID monitor circuit are active. When Vid=0V, AK8963 is in reset status and it consumes the current of reset state (IDD4).

AK8963 has four types of reset;

- (1) Power on reset (POR)  
When Vdd rise is detected, POR circuit operates, and AK8963 is reset.
- (2) VID monitor  
When Vid is turned OFF (0V), AK8963 is reset.
- (3) Reset pin (RSTN)  
AK8963 is reset by Reset pin. When Reset pin is not used, connect to VID.
- (4) Soft reset  
AK8963 is reset by setting SRST bit.

When AK8963 is reset, all registers are initialized and AK8963 transits to Power-down mode.

### 6.3. Operation Modes

AK8963 has following seven operation modes:

- (1) Power-down mode
- (2) Single measurement mode
- (3) Continuous measurement mode 1
- (4) Continuous measurement mode 2
- (5) External trigger measurement mode
- (6) Self-test mode
- (7) Fuse ROM access mode

By setting CNTL1 register MODE[3:0] bits, the operation set for each mode is started. A transition from one mode to another is shown below.

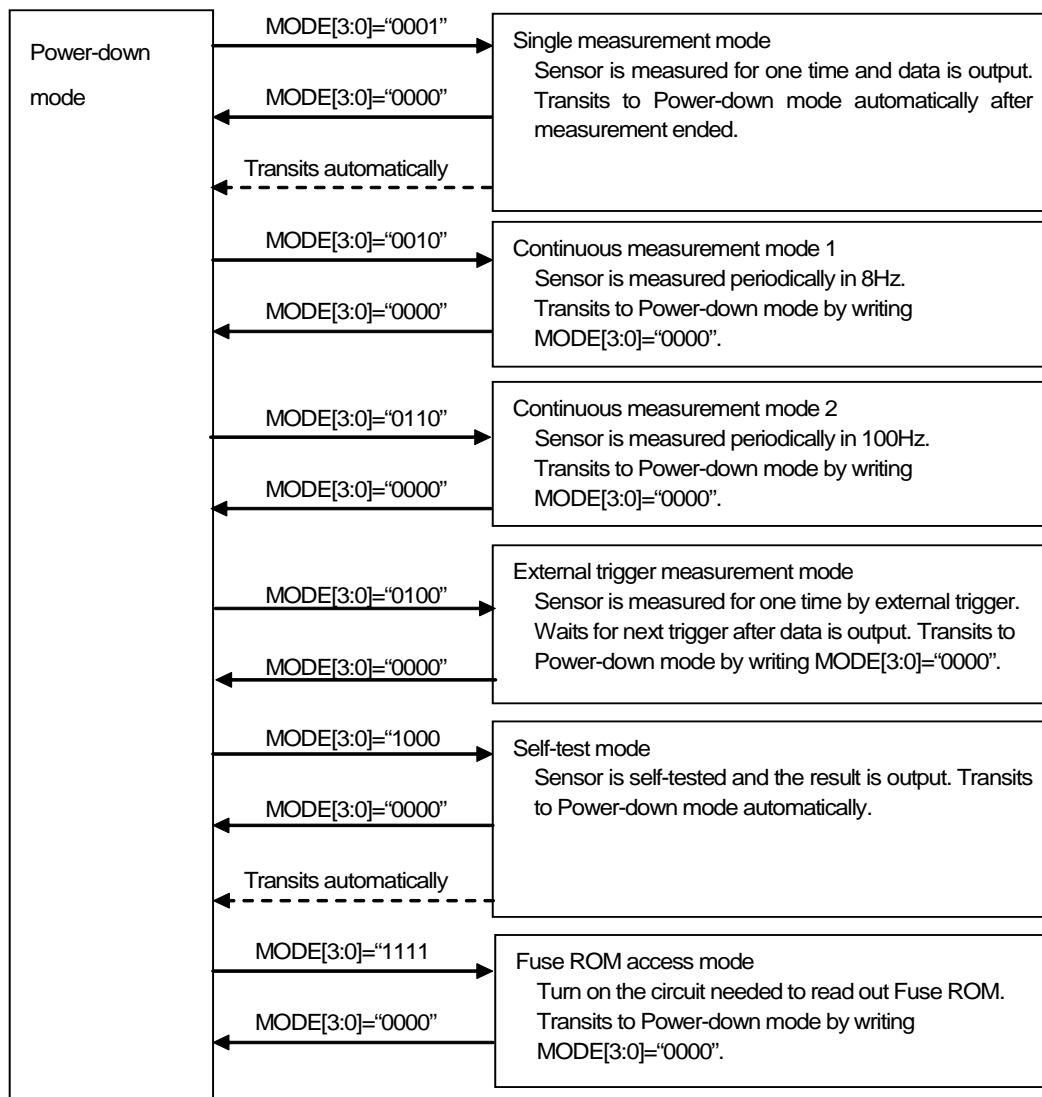


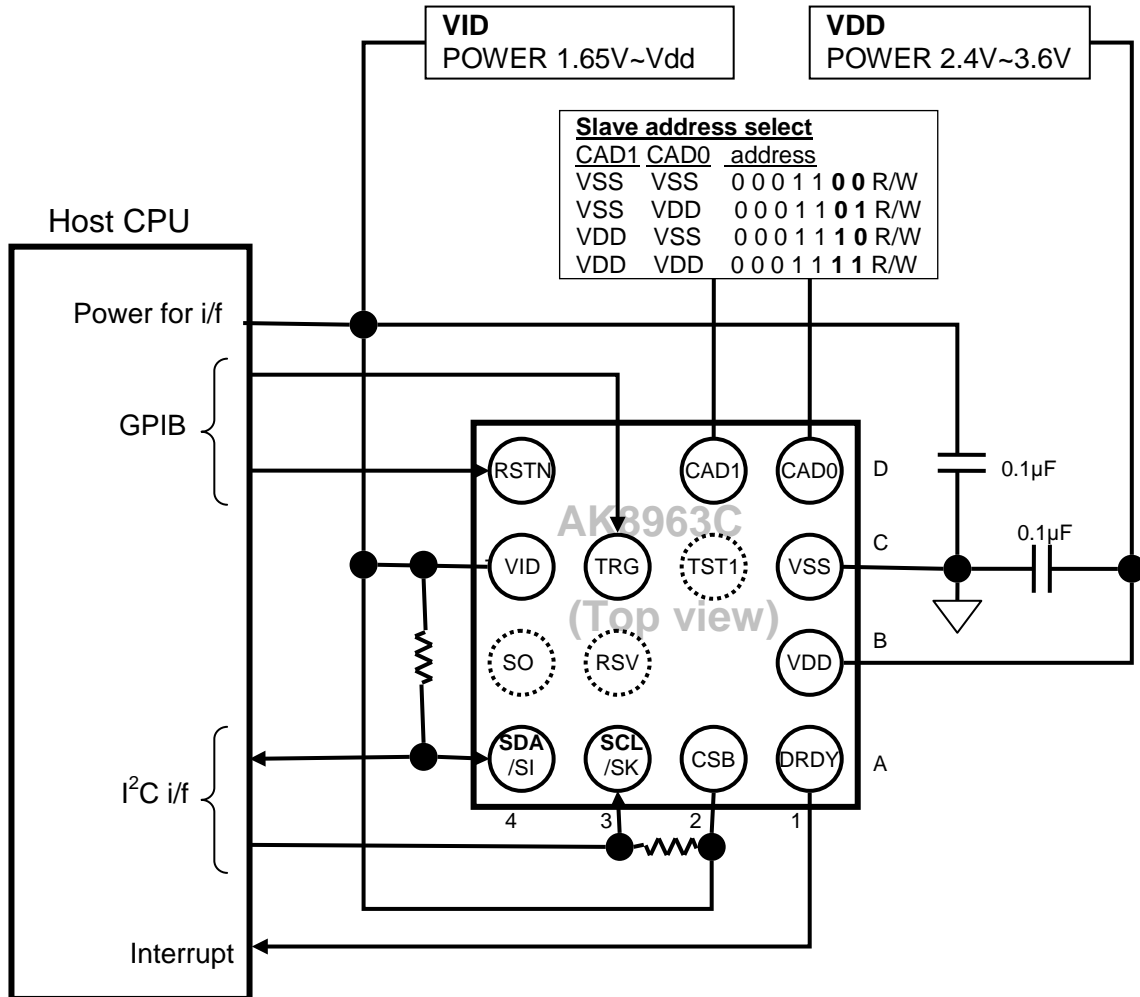
Figure 6.1 Operation modes

When power is turned ON, AK8963 is in power-down mode. When a specified value is set to MODE[3:0], AK8963 transits to the specified mode and starts operation. When user wants to change operation mode, transit to power-down mode first and then transit to other modes. After power-down mode is set, at least 100ms (T<sub>wait</sub>) is needed before setting another mode.

## 7. Example of Recommended External Connection

### 7.1. I<sup>2</sup>C Bus Interface

<AK8963C>



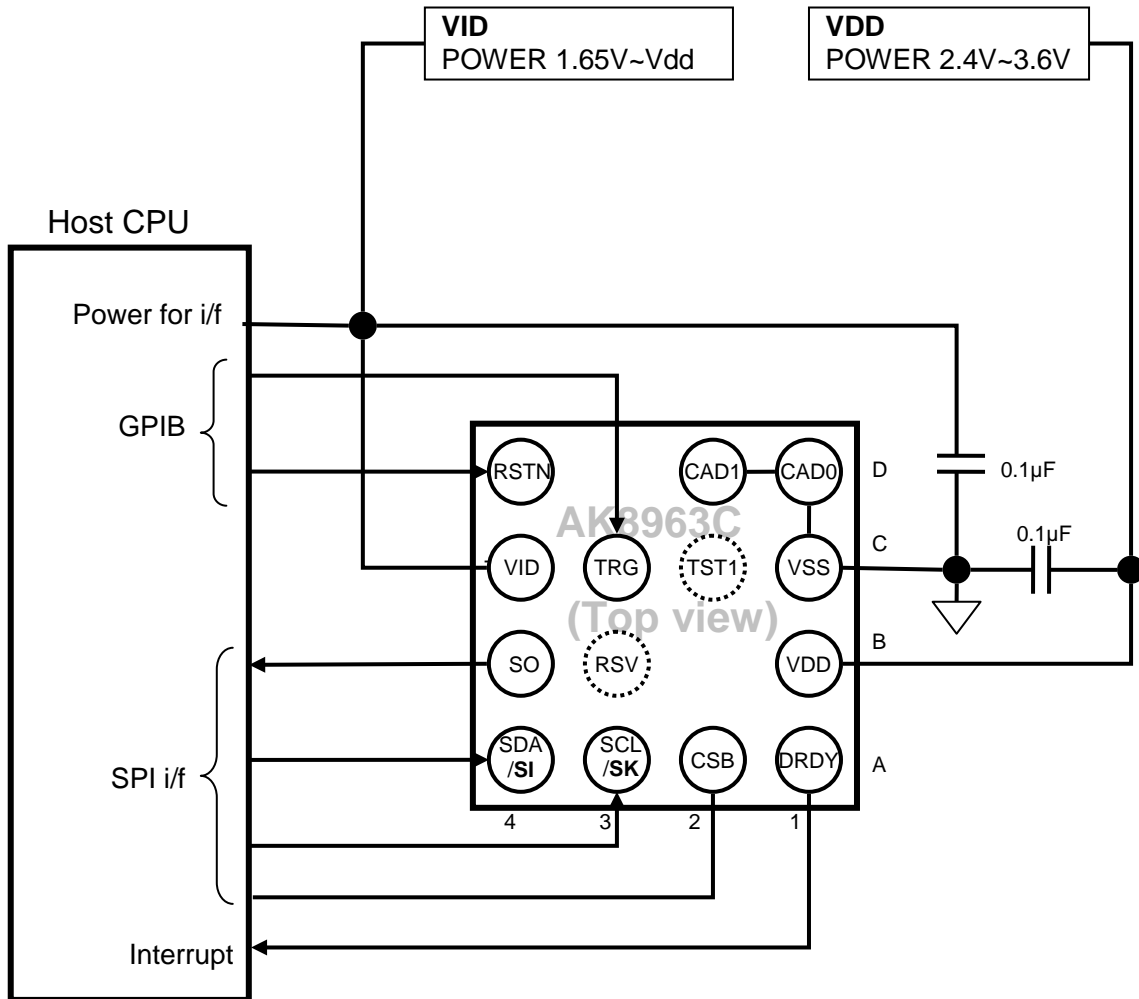
Pins of dot circle should be kept non-connected.

<AK8963N>

Same as AK8963C.

7.2. 4-wire SPI

<AK8963C>



Pins of dot circle should be kept non-connected.

<AK8963N>

Same as AK8963C.

# 8. Package

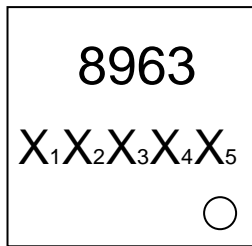
## 8.1. Marking

<AK8963C>

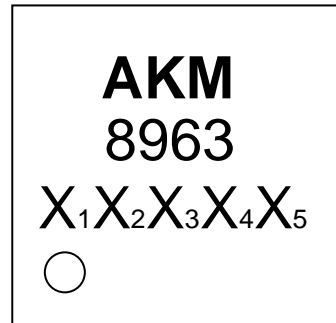
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- Date code: X<sub>1</sub>X<sub>2</sub>X<sub>3</sub>X<sub>4</sub>X<sub>5</sub>
  - X<sub>1</sub> = ID
  - X<sub>2</sub> = Year code
  - X<sub>3</sub>X<sub>4</sub> = Week code
  - X<sub>5</sub> = Lot

<AK8963N>

- Company logo: AKM
- Product name: 8963
- Date code: X<sub>1</sub>X<sub>2</sub>X<sub>3</sub>X<sub>4</sub>X<sub>5</sub>
  - X<sub>1</sub> = ID
  - X<sub>2</sub> = Year code
  - X<sub>3</sub>X<sub>4</sub> = Week code
  - X<sub>5</sub> = Lot



<Top view>



<Top view>

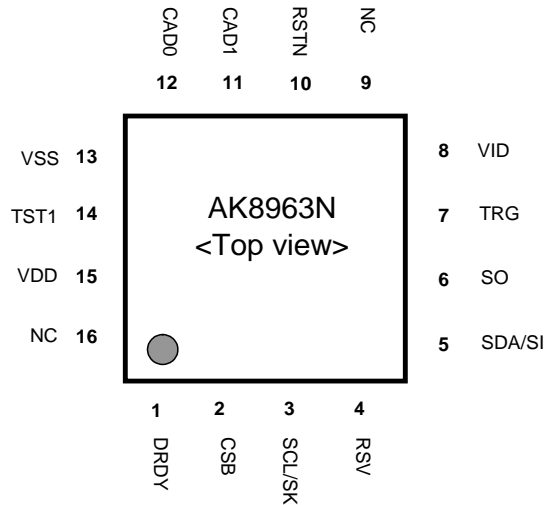
## 8.2. Pin Assignment

<AK8963C>

	4	3	2	1
D	RSTN	/	CAD1	CAD0
C	VID	TRG	TST1	VSS
B	SO	RSV	/	VDD
A	SDA/SI	SCL/SK	CSB	DRDY

<Top view>

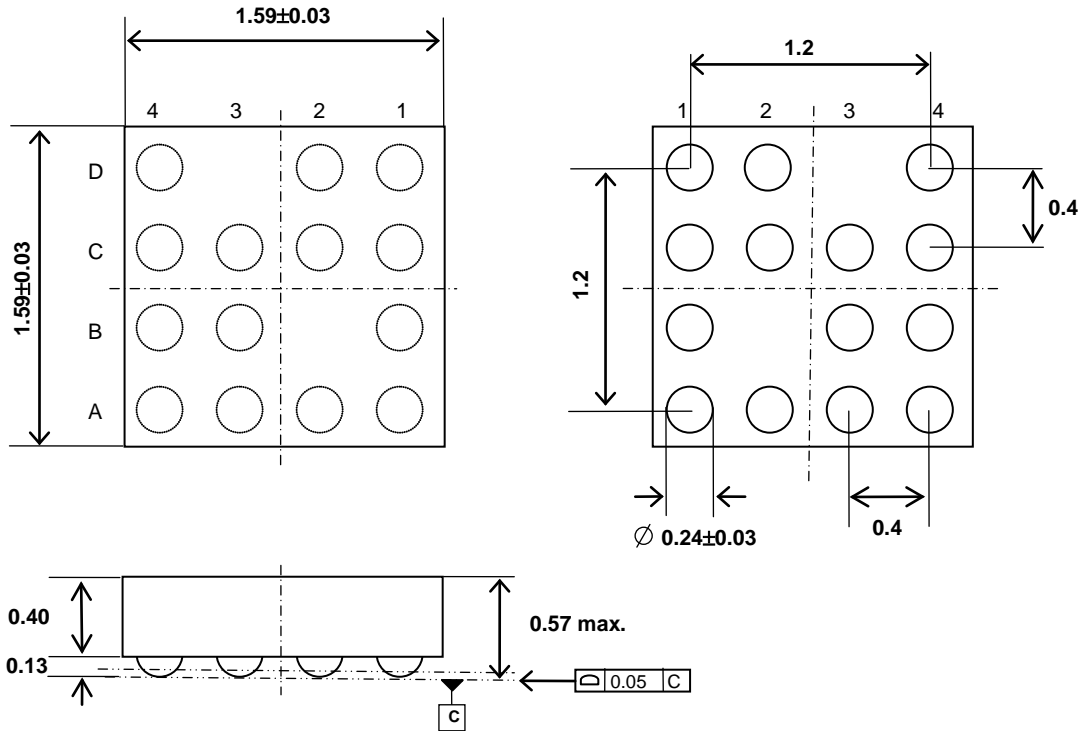
<AK8963N>



8.3. Outline Dimensions

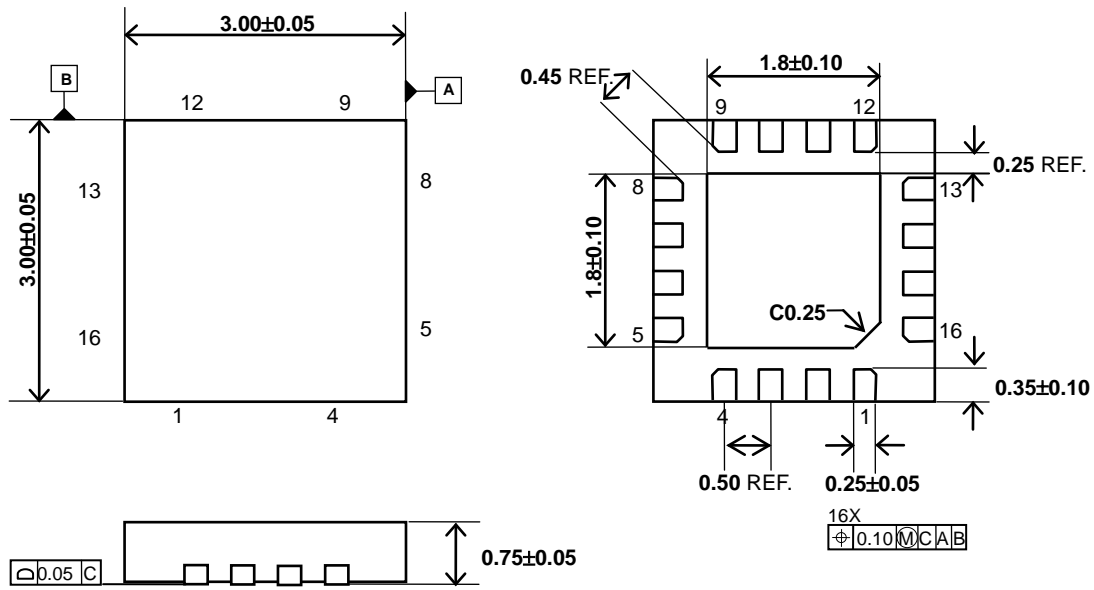
<AK8963C>

[mm]



<AK8963N>

[mm]

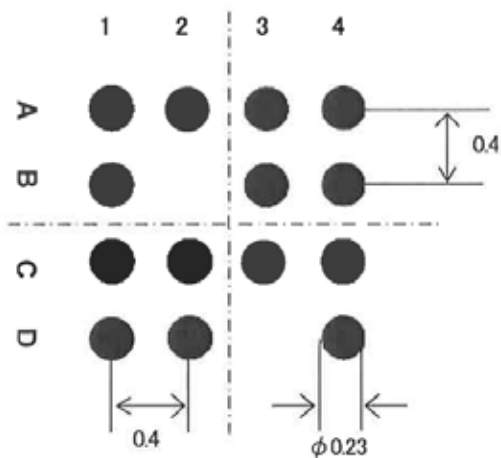




8.4. Recommended Foot Print Pattern

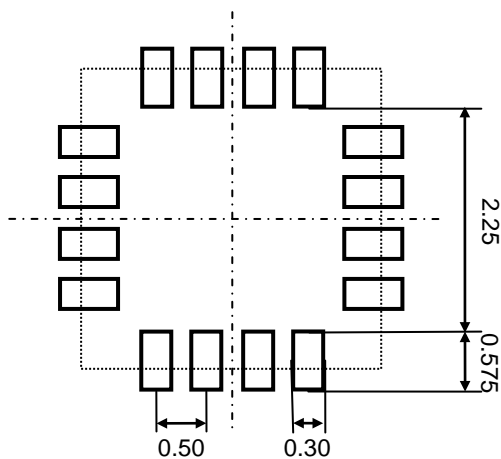
<AK8963C>

[mm]



<AK8963N>

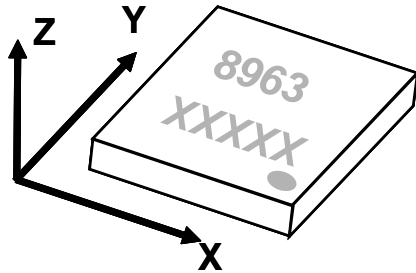
[mm]



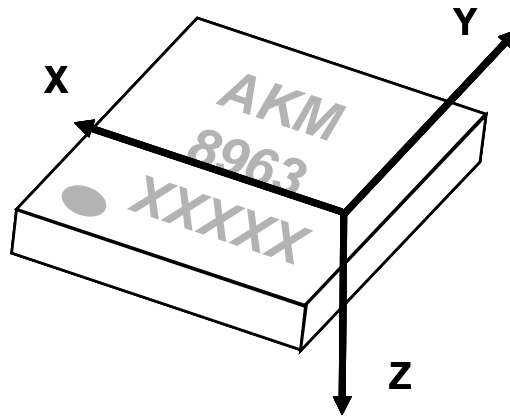
## 9. Relationship between the Magnetic Field and Output Code

The measurement data increases as the magnetic flux density increases in the arrow directions.

<AK8963C>



<AK8963N>



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