APPLICATION NOTE

Product Name	M500 802.11b/g/n, BT 2.1+EDR, FM Rx, GPS SiP 4-in-1 Module
Version	A
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Document History

Date	Revise Contents	Revise by	Version
Sep. 27th , 2012		Kenny	1.0
Sep. 28th , 2012	Modify Application Circuit	Kenny	1.1
Jan. 04th , 2013	Modify Application Circuit & add Recommended Footprint	Kenny	A

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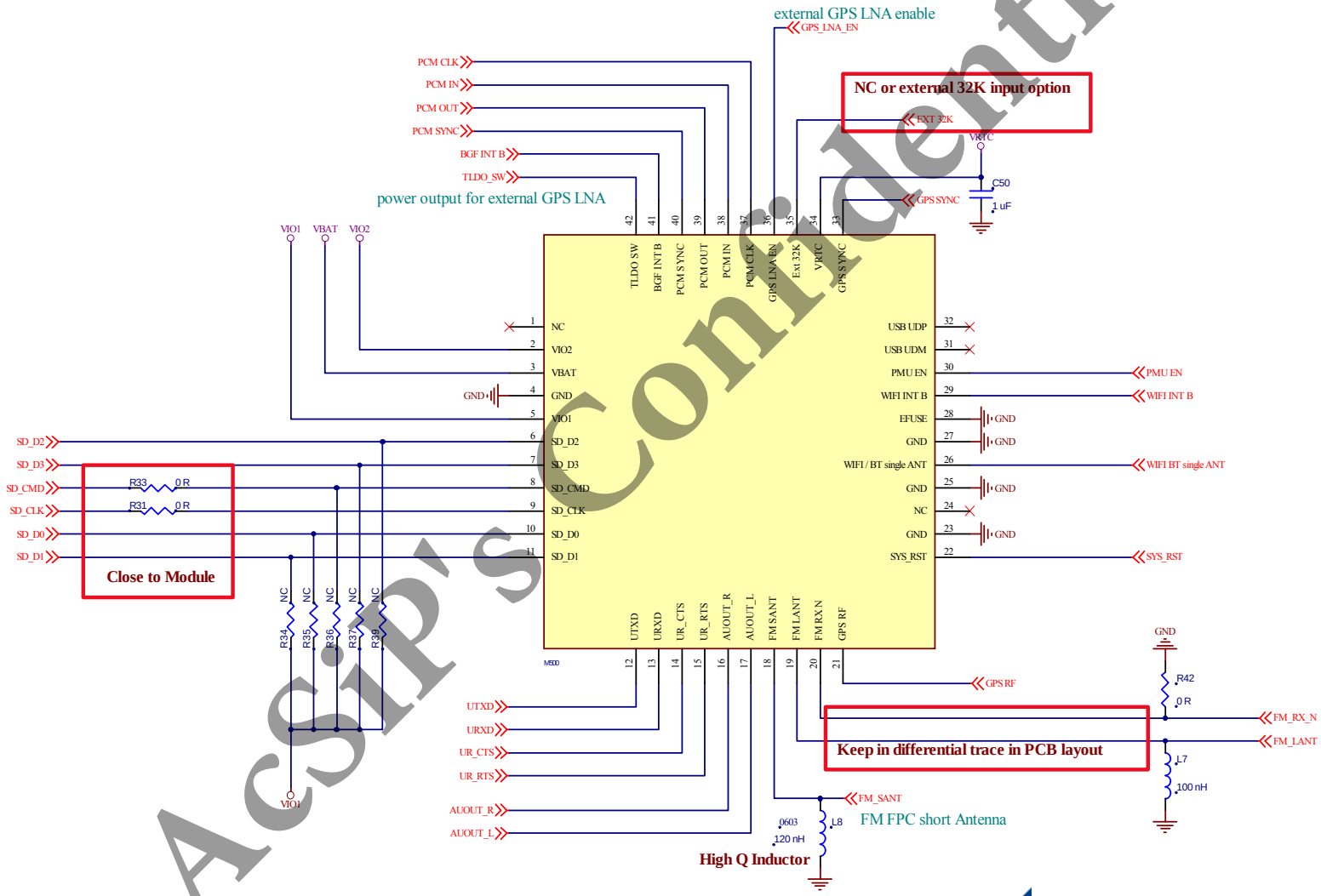
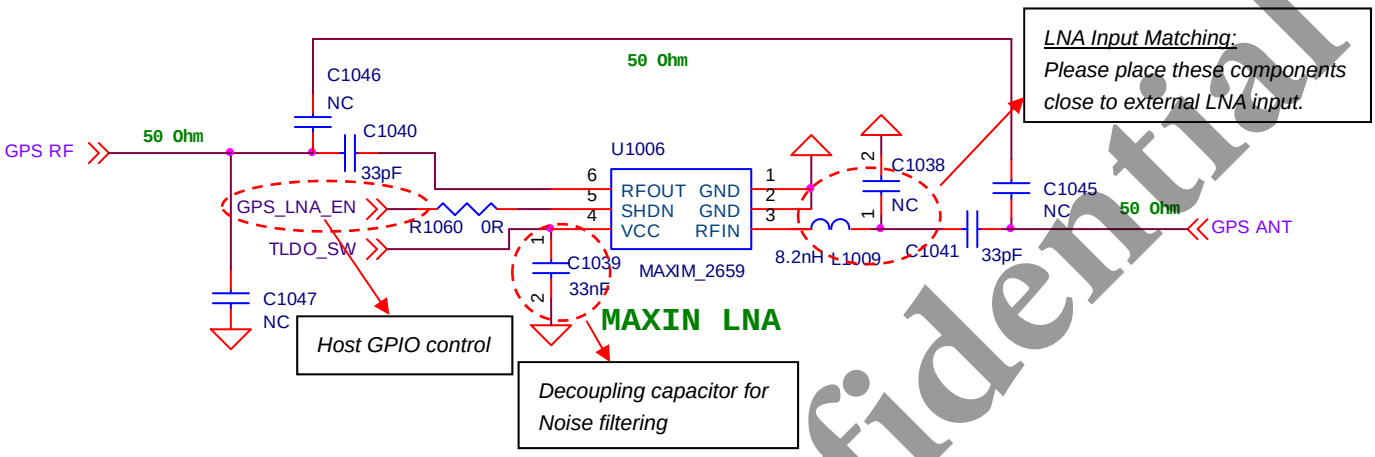
1. Application Circuit

1-1. M500 reference design



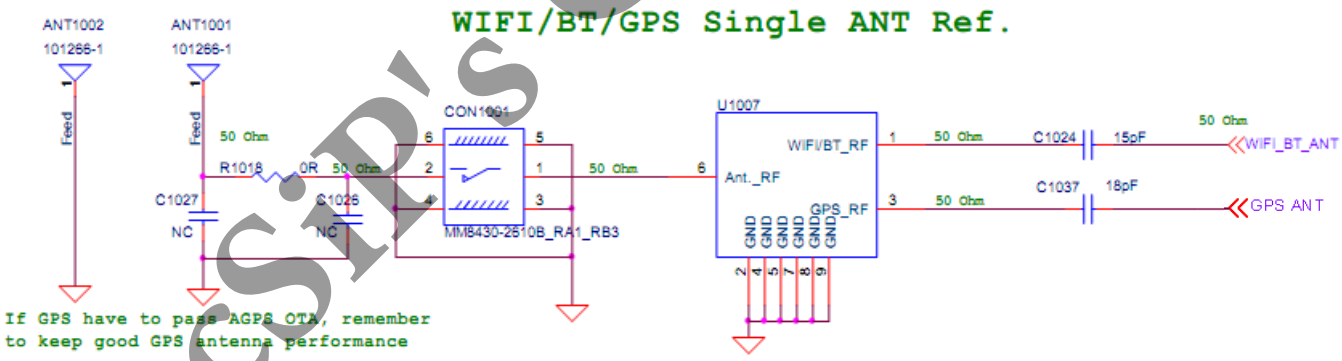
1-2. External LNA for GPS

- Use host GPIO (recommended) or GPS_LNA_EN to control GPS external LNA enable pin.
- Place decoupling capacitor to close to external LNA power pin.
- Place matching components close to external LNA input.



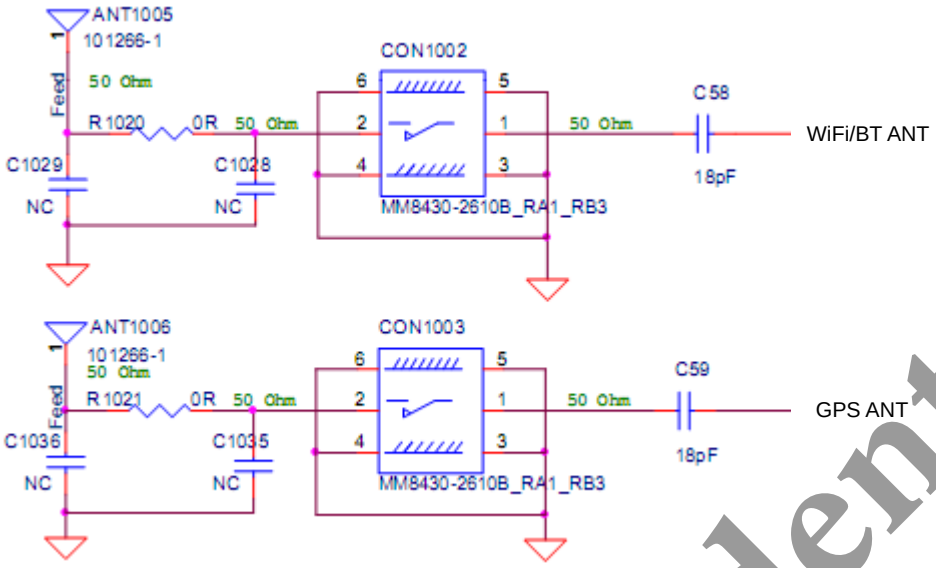
(Optional) external LNA for better GPS performance

1-3. WiFi / BT & GPS single antenna



(Optional) reserve L=39nH at C1026 for ESD protection

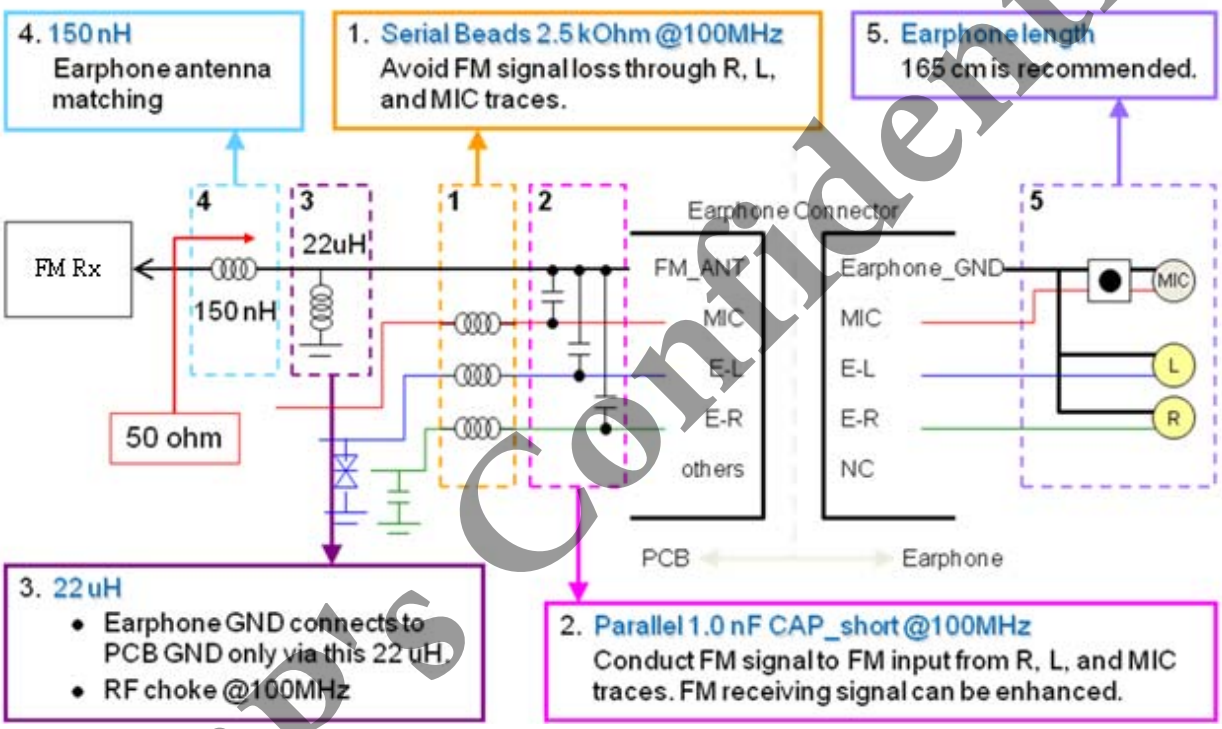
1-4. WiFi / BT & GPS dual antenna



(Optional) reserve L=39nH at C1028 / C1035 for ESD protection

1-5. FM audio jack / antenna

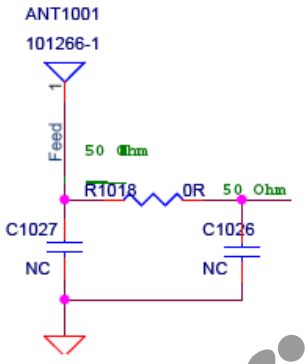
- Add a LPF(chip out series 27nH, than parallel 10pF) on FM long Antenna trace, for WLAN/BT out band blocking de-sense.
- Keep FM Antenna(audio jack/ usb / FPC) and RF traces away from power source and other Antenna like WLAN/BT/GSM Antenna, to avoid de-sense.
- RF Traces should be far away and well- grounded from VBAT / VDDK and any other VDD traces.
- VFM trace should be well ground shielding.



1-6. Application Note

The M500 module supports SDIO interface for WiFi, UART for Bluetooth, FM, GPS.

- π-network is reserved for antenna matching. The π-network's value in the application circuit can be configurable.



2. Layout Guide

2-1. Power Line Management

- The let power lines should be directly connected with regulator outputs, and adds 1uF bypass capacitors close to module on each power line.
- Never let power trace cross the other one including signal trace.

2-2. 32kHz Clock Management (optional)

- The 32KHz signal trace couldn't be mixed with any power line, and avoid any signal trace close to 32KHz signal trace.

2-3. SDIO Bus

- Please reserve damping resisters on SDIO_CMD and SDIO_CLK and place them close to module for optimizing SDIO performance.
- Make SDIO_CLK, CMD and Data in a layout group.
- SDIO_CLK is a high speed signal and it must be shielded by GND plan for reducing noise. And don't mix then with other trace.

2-4. Ground Management

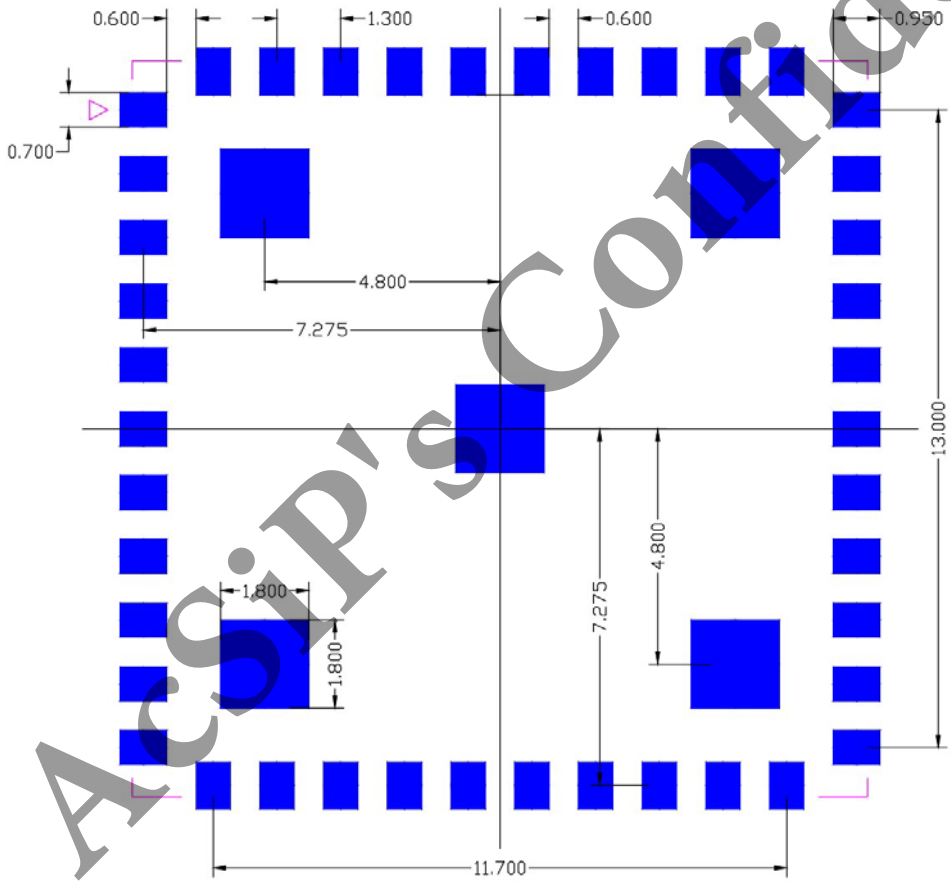
- Please ensure the regional first layer used to mount module is complete to the ground.
- The ground plane on both sides of RF trace needs to add via holes and. We recommend the distance between adding via holes less than 1/8λ.

2-5. RF Trace Management

- CPWG-type traces used for RF function are recommended, which having better EMC and RF capability.

2-6. Recommended Footprint

(TOP VIEW)



UNIT: mm

3. The Other Information

- Do not put any signal line or power line on system PCB top layer under M500 module.
- Discuss with AcSiPs' engineer after schematic and layout finished.